2006-77: INTRODUCTORY MEMS TECHNOLOGY USING BULK MICROMACHINING IN THE SEMICONDUCTOR MANUFACTURING CURRICULUM

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Introductory MEMS technology using Bulk Micromachining in the Semiconductor Manufacturing Curriculum

I. Introduction

Microelectromechanical systems (MEMS) are small, integrated devices or systems that combine electrical and mechanical components. They range in size from sub micrometer (or sub micron) to millimeter. MEMS extends the fabrication techniques developed for integrated circuit industry to micromachining and manufacturing by adding mechanical elements such as beams, gears, diaphragms, and springs to devices. These systems can sense, control, and activate mechanical processes on the micro scale, and function individually or in arrays to generate effects on the macro scale. Consequently, the micro fabrication technology enables fabrication of large arrays of devices, which individually perform simple tasks, but in combination can accomplish complicated functions[1].

Although MEMS is relatively a new technology introduced in industry, significant teaching potential of introductory MEMS technology is identified in the Semiconductor Manufacturing Technology (SMT) curriculum. The SMT class (TECH4392) taught at Engineering and Technology Department covers broad spectrum of SMT technologies from the crystallographic structure of the silicon substrate to IC inspection. It consists of 5 lab sessions of semiconductor fabrication in the class 10,000 cleanroom in the department. Primary lab activities include silicon oxide growth, aluminum PVD (Physical Vapor Deposition), photolithography, etching and surface inspection.

To introduce fundamentals of MEMS technology in SMT class, we used statements by leading researchers such as Kaigham (Ken) J. Gabriel, a Carnegie Mellon University professor who illustrates the fabrication of MEMS simply as “we deposit materials and remove them,” essentially the same as ICs manufacturing process. However, “the films put down are thicker by an order of magnitude,” he added. These films can grow several microns thick, sometimes up to 10 microns, while IC thin-film layers are typically measured in angstroms these days. In addition, MEMS fabrication calls for deeper etches. “The whole point of MEMS is to wind up with a mechanical structure that moves,” said Gabriel, who once led the DARPA MEMS program[3]. These remarks unveil any fear or hesitation on the part of students and allow us to introduce a whole new area of study different from the main class curriculum, but at the same time similar in many manufacturing aspects.

In spring 2005, a group of students who registered in TECH4392 for research credits went through entire bulk micromachining processes from design to fabrication (in section III). While taking the SMT course, they reported their works at each significant milestone and provided full presentation at the end of the semester. Due to the analogy in terminologies and processes between MEMS technology and SMT, students in two different groups seem to experience minimal difficulties for teaching and communication. In order to introduce the fundamentals of the MEMS technology in the SMT curriculum, a bulk micromachining process of pure silicon is considered. Although brittle in macro scale, Si has higher intrinsic yield strength (7 Gpa) than steel (4.2 Gpa), thus often being considered for micro structure fabrication material such as beam or gear structures[6]. In this paper, we share detail processes and process parameters for Si fabrication by students.

As for the paper structure, this paper is composed of three sections: Bulk micromachining overview, Experimental results, and conclusion. Significant portions of this paper are dedicated to students' works and experimental results shared in the class. The target structure fabricated during the semester is a silicon cantilever beam structure for air pressure sensor manufacturing. Most often sited source for the bulk micromachining process is the polysilicon surface micromachining research studied at the University of Wisconsin at Madison.

II. Bulk Micromachining Process

While most chemical etching processes in SMT are isotropic and largely used for etchback (complete surface removal) or surface cleaning, some are known to be anisotropic suitable for precision microstructure manufacturing. For instance, KOH is a chemical compound that attacks silicon, producing characteristic anisotropic V-etch, with sidewalls that form a 54.7° angle with the surface (35.3° from the normal). This etch process is independent of the doping concentration of As, P and Sb. For B, the <110> etch rate drops quickly at high doping concentrations though. Such precision V-etch by selective wet etching is the foundation of the bulk micromachining.

The two key capabilities that lead bulk micromachining to become a viable technology in MEMS are: (1) Anisotropic etchants of Si, such as ethylene-diamine and pyrocatechol (EDP), potassium hydroxide (KOH), and hydrazine (N_2H_4); and (2) Etch masks and etch-stop techniques that can be used with etchants to selectively prevent regions of Si from being etched. Good etch masks commonly used are SiO_2 and Si_3N_4, and some metallic thin films such as Cr and Au (gold)[1]. In the fabrication of MEMS components, thick resist coatings are often applied during wafer processing[7]. Deeply etched silicon structures are formed by plasma[8] or wet anisotropic etching in alkali etchants such as KOH[9]. It is known that KOH reacts to pure silicon discriminately depending on the crystal direction. KOH solutions react to <110>:<100>:<111> planes selectivity in the etching rate as high as 600:400:1 and provides etch rates of up to 2 micon/min with good selectivity for oxide, nitride, and other etch stop regions[9]. It is this capability of selective etching that enables the etchant to shape the silicon substrate to various useful patterns.

High-aspect-ratio microstructures formed by these processes have proven to be particularly difficult to measure by conventional methods. Such micromachined structures often exceed 100 *m*in height. These structures are much larger than IC critical dimensions, which are typically measured by stylus profiling, yet significantly smaller than conventional metal-machined parts, typically measured by mechanical gauges and other machine shop instruments[5]. In this project, students used digital photo imaging technique to measure critical dimensions of final products to discuss results of the developed process.

In the following section, some significant milestones shared and presented during the semester are detailed. In the experiments, <110> pure silicon wafer is used for cantilever beam structure fabrication.

III Experimental results shared in the SMT course

In this section, we present some significant milestones shared in the class by a group of students who went over the micro-beam structure fabrication.

Cantilever Beam Design

Sensor Design: Due to process limitations, our cantilever pressure sensor will consist of a flat Si layer, which will make up the entirety of the mechanical structure (Figure 1, Figure 2). The 0.5mm thickness of the wafer will dictate that we need to remove the silicon layer completely due to the angle of the anisotropic etching and the desired size of the device. The smallest cantilever beam for the sensor is 300 microns wide and 1,270 microns tall, while the pressure sensing head is a rectangle of 600 by 450 microns.

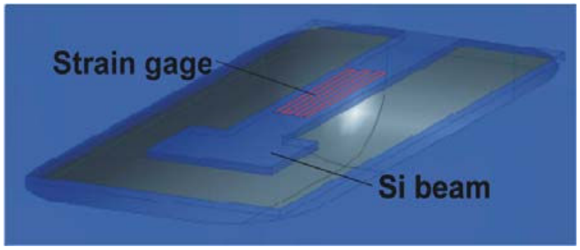

Figure 1: Ideal sensor design

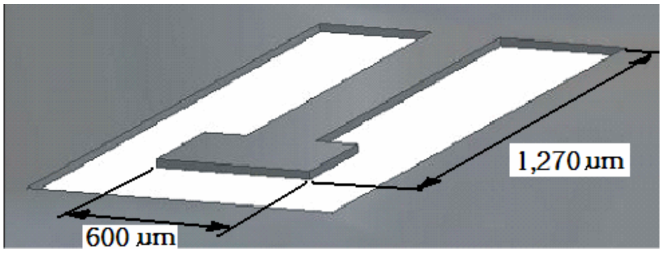

Figure 2: Beam design

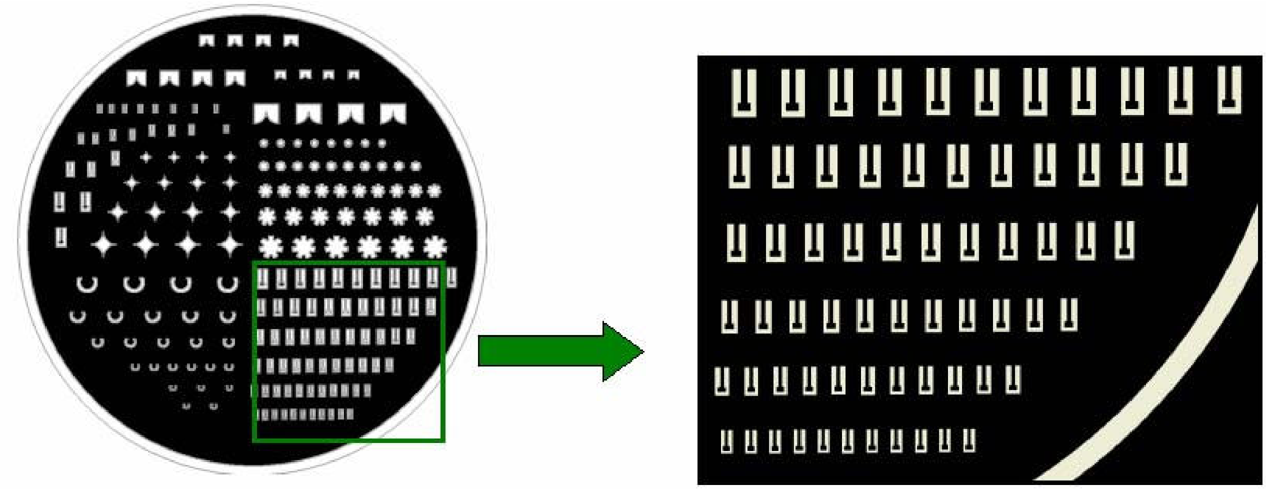

Figure 3: Photomask

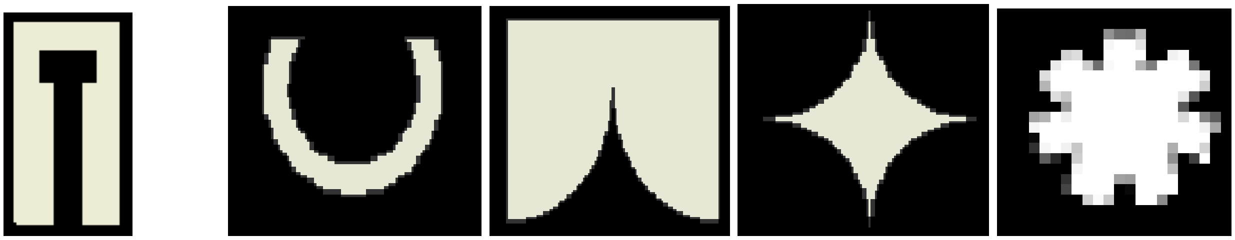

Figure 4: Cantilever sensor with other test geometries

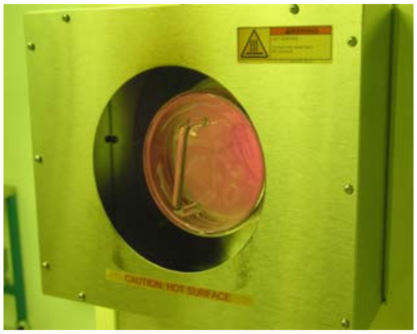

Figure 5: Oxidation furnace device

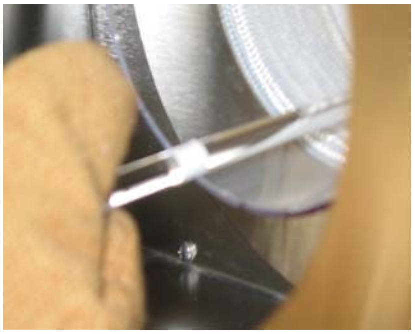

Figure 6: Pyrex rod w/ depth mark

Figure 7:Mask reduction

Figure 8: Spinner

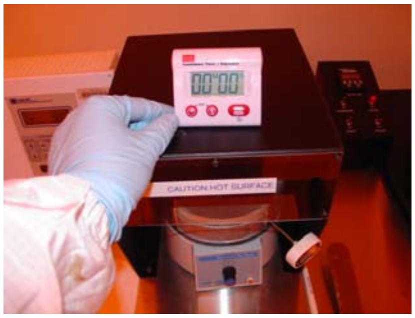

Figure 9:Soft baker

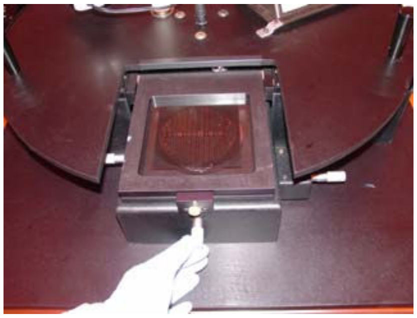

Figure 10: Contact mask aligner

The Photomask: The photomask is consisted of a gradient of 60 different device dies varying in size from 40 *mm* to about 1,500 microns tall. Also included in the design are several different die shapes of different sizes to test the process capabilities and examine how the KOH cleaves along the crystal planes (Figure 3, Figure 4). The geometry has been designed such that the undesired but inevitable etch of SiO_2 by the KOH will leave enough material to form a beam.

Siliconoxide layer deposition

The first process necessary for micro-pressure sensor is to grow siliconoxide layer. The target thickness of the silicon oxide is ~10,000Å and the starting temperature in the furnace (Figure 5) is set to be 750° F. We then purge the gas lines with O_2 and N_2 at 20psi from the source canisters. To begin the process, we employ the Nitrogen to push out the Oxygen from the furnace to better control the reaction. Once the desired starting temperature is reached and the O_2 is purged from the furnace, we then place the wafer boat in the furnace using a Pyrex rod marked with the proper depth for best growing condition (Figure 6). Once the wafer boat is in the furnace, we increase the temperature to 1,000° F. When the reaction temperature is reached, we introduce the oxygen at Level 4 on the flow meter on the right side of the furnace (approximately 1.24 *l* per minute).

Photolithography

Lithography is a process whereby a pattern on a mask is transferred to the film by means of a photosensitive (i.e., light sensitive) chemical known as a photoresist. The process of pattern generation and transfer is called photolithography. A typical mask consists of a glass plate coated with a patterned chromium (Cr) film[1]. The photoresist will protect selected areas of the underlying SiO_2 layer from the Hydrofluoric acid (HF) etching process. For our creation of the photomask we took the designed template with all the device geometries laid out and printed at 32" x 32" (for increased resolution), and reduced it to the size of a wafer (Figure 7). We then moved the wafer and the mask into a darkroom for the remaining lithography processes. First, we cleaned the wafer and mounted it on a programmable spinner (Figure 8). Then, we slowly applied 2*ml* of photoresist to the center of the wafer, followed by a programmed spinning cycle. After the wafer had adequate coverage of photoresist throughout the surface, we removed the solvents from the photoresist by placing it in the micro-oven for 90-120 seconds (Figure 9). After the softbake, the wafer was ready for exposure. The most critical factor in the photolithography process is to ensure the accuracy of positioning the photomask in the contact mask aligner (Figure 10). Once correctly positioned, we exposed the wafer to UV light for 150 seconds, followed by development in a bath.

SiO_2 Etch

The next step in the process is the selective removal of unwanted regions of the silicon substrate for pattern formation. Wet chemical etching or dry etching may be used. Etch-mask materials are used at various stages in the removal process to selectively etch only those areas planned for removal. Examples of etch-mask materials include SiO_2, Si_3N_4, and hard-baked photoresist[1].

With the layer of photoresist completely exposed and developed, we then used Buffered Oxide Etch (BOE) to etch the wafer. The wet etch process took about 25 minutes. The evidence of a successful etch can be measured by the hydrophobic/hydrophilic properties of the wafer surface, since the unexposed portions of the wafer repel water whereas the openings in the SiO_2 hold water. The result can be further verified by examination through a microscope. At the sharp corners of the geometry of the device there was a "rounding" effect. Also noticeable was an estimated 5% degradation of the device geometry due to the inaccuracy of the lithography equipment and process.

Anisotropic Wet Etching or Bulk Micromachining of Silicon

Once the openings of the SiO_2 were made clear, we used KOH to attack pure SI layer for micro structure sculpturing. For our experiment, 45% KOH was prepared with a mix of water and isopropyl alcohol. The KOH etch requires a "hard mask" of silicon dioxide or silicon nitride (nitride is preferred since oxide is slowly etched by KOH). While the etching occurs, it is vital that the process be closely monitored to maintain uniform etching. Additional heat promotes the etching rate, creating convection currents in the KOH solution. At 80 degrees C, the etch rate of <100> *Si* is about 60 microns/hour, while SiO_2 is at 420 nm/hour[9]. Since we had a 0.5mm thick silicon substrate, the estimated period for designed beam structure was about 4.5 hours.

Results

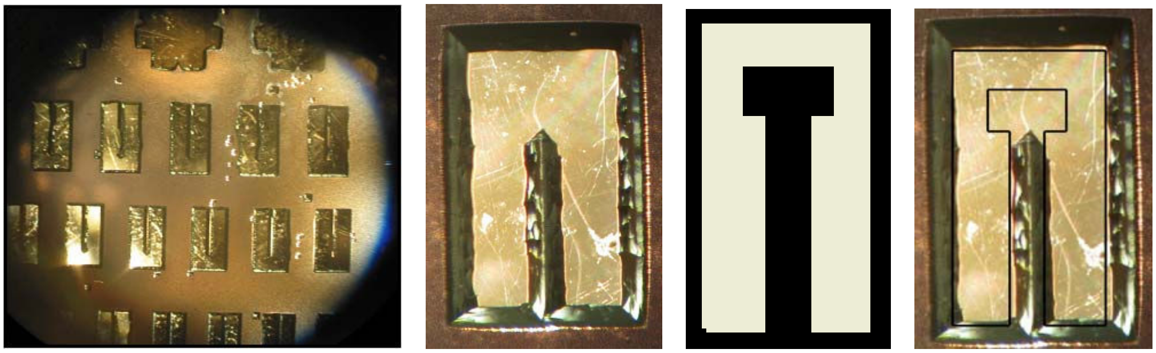

Figure 11: from left to right: 1. device array, 2. a single device, 3. the original design, 4. superimposition of completed device and original design

To analyze experimental results for class presentation and useful information with respect to future design considerations, we employed an optical approach, where the general outside dimensions are measured with the pictures of the microscopic devices, and the known geometries of the photomask are compared to the picture (see Figure 11). Other patterns assured that the sharp corners cannot be fabricated unless they are within crystal angle of the *Si* substrate.

From the geometric analysis we found:

- ~7.74% degradation of overall opening
- Lever head totally etched away
- 54.7° sidewalls
- ~300 micron lever width
- 19.4% reduction in lever length

From the expected results:

- 5,000,000Å substrate at an etch rate of (2x) 550,000Å per hour yields a 4.5 hours etch time to etch substrate completely
- 10,000Å Oxide Layer at an etch rate of 2,000Å per hour for 4.5 hours yields a 1,000Å thick device.

Using simple trigonometry knowing the etch angle from the KOH, anisotropic process yields

$$1,279\overset{\circ}{A}(width) = 2\times\tan(32.6)\times 1,000$$

Thus, the minimum device width allowed by this process is ideally 1,279Å.

III. Conclusion

In order to introduce the results of the MEMS fabrication study, a series of presentations is prepared and shared by students. First, at each milestone, students gave presentation as well as final presentation at the end of the semester. In the final presentation, the introduction of MEMS technology is presented by a lecturer followed by the detail design and process summary of the bulk micro-etching by students. During the presentation of the experimental results, emphasis was made on MEMS design, equipment requirements, and process of each fabrication step. At the end of the semester, the audiences were expected to be aware of fundamental semiconductor fabrication technologies along with equipments required at the different stages.

Although MEMS is a new emerging research area, the majority of audiences in the class seem to have impression that the cutting edge MEMS technology is not far different from what they have learned in the SMT class. Pedagogically, it was evident that the use of similarities in two different areas of studies made it easy to draw attention of students. In addition, experimental activities not only motivated students but also boosted learning process with longer memory retention. For instance, in the presentation, presenters well defended questions from audience conveying details of processes of each fabrication stage.

As a result, it was evident that the fundamentals of emerging MEMS technology can be taught in an undergraduate curriculum effectively. The bulk micro-etching of pure silicon was selected as a vehicle to convey the technical aspects of MEMS in the class. It also provided an entire spectrum of research experiences from design, data collection, analysis, to charting, illustration, presentation of experimental results. Course surveys at the end of the 2005 spring semester revealed that majority of students desire to take a subsequent class focused more on advanced semiconductor fabrication and MEMS technology.

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