

Minimum Inventory Variability Dispatching Policies - MIVP[®]

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Abstract

This paper illustrates the use of discrete event stochastic simulation modeling to compare two scheduling (dispatching) policies for machines in a factory when a machine becomes available for processing. The two policies are first-in-first-out (FIFO) and Minimum Inventory Variability Policies[®] (MIVP[®]), both control the items in the queue (buffers) in front of the machine or resource^{8,9,10,11}. The simulation model is run with FIFO for each queue for 100 days to establish a baseline set of data. This baseline cycle time and work-in-progress (WIP) data are collected for comparison to MIVP[®]. The only change between the model runs is that the queues in the model are switched to run the rule set of MIVP[®].

With discrete event simulation modeling, the user can play “what if” scenarios without expended a lot of capital^{4,5,8,9,10,11,19,20}. The results from simulation give the user an additional input in making decisions. Examples of such a simulator use include the analysis of machine utilization, queue statistics, mean cycle time and mean WIP and production throughput, etc. This analysis can serve to push the bottleneck capacity to its limit, setup and test scheduling rules and preventive maintenance schedules, and determine personnel (operator) availability requirements. Thus, a good simulator allows for the investigation of complex “what-if” scenarios at a minimal cost, high speed, and without disturbing the normal production.

The System Model

The following figure and specification was taken from a test-bed designed by Karl Kempf, Manufacturing Systems Principal Scientist, of the INTEL Corporation. This test-bed is an example of a very small section in the Semiconductor FAB and is referred to as a Mini-FAB^{6,14,16}.

The Mini-FAB included two products and test wafers with their process flows (production recipes) of six steps utilizing three different machine sets. There was one re-entrant step at each machine group, steps 4, 5 and 6. The machine groups emulate (in a small scale) Diffusion-C1 (2

machines Ma and Mb), Implant-C2 (2 machines Mc and Md) and Photolithography-C3 (1 machine Me).

Machines Ma and Mb in the Diffusion bay used predictive machine controllers (a PID controller compared to an H-infinity controller)^{11,20} to establish when the machines were to be taken down for emergency maintenance. Predictive controllers are being researched for yield improvement to determine a potential failure prior to its occurrence so the product being processed is not scrapped^{7,11,13,17,18,19,20}. Machines Mc and Md in the Implant bay used historical data of Mean-Time-Before-Failure (MTBF) and Mean-Time-To-Repair (MTTR) as the emergency maintenance. All machines had a specific Preventive Maintenance Schedule (PM) with rules for when the machines could be taken off line for PM.

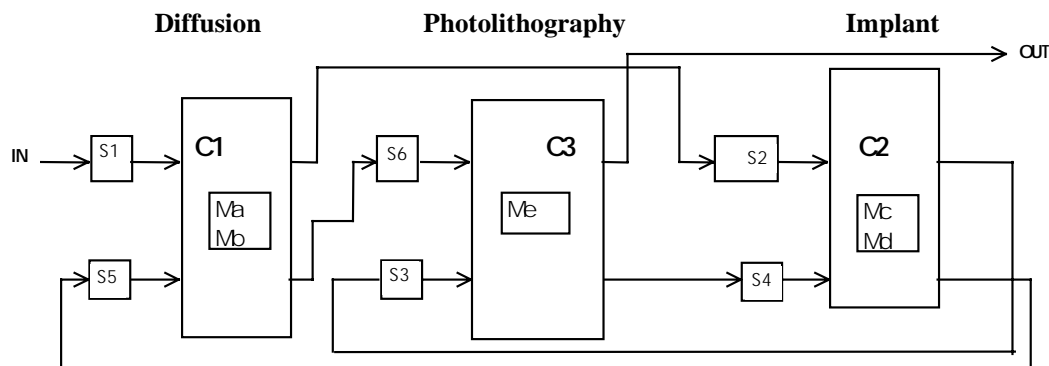


Figure 1. Schematic diagram of the 5 machines 6 steps process flow¹¹

The objective of this study is to compare Minimum Inventory Variability Policies[®] - MIVP[®] queue-machine dispatching policy to the first-in-first-out (FIFO) dispatching policy for the Mini-FAB example. The MIVP[®] decreased cycle time by 19% when compared to FIFO¹¹. This example demonstrates an advantage of MIVP[®] over FIFO even in the small number of process steps and machine groups. The advantage of MIVP[®] becomes more pronounced in manufacturing problems with multiple products with large number of process steps, many machine groups and multiple reentrant levels. For example, typical semiconductor operations involve 300+ average steps, 130+ parallel machine groups and 15+ layers on the wafer. A recent implementation of MIVP[®] in a real Semiconductor-FAB with 55 different micro-controller devices has seen a decrease in product average cycle time of 32.9% (reducing from 49 days to 31 days in less than six months). The average process flow, in this FAB, of each device was 285 steps (from 164 steps to 350 steps) with reentrant levels averaging 10 layers on the wafer. The FAB included 132 machine groups (with 485 machines). This reduction was evaluated at \$100+ million US savings per year^{8,9}.

The MIVP[®] set of heuristic rules looks at the queue wait time at every resource in the factory and not just at the known bottleneck sections of the FAB. MIVP[®] enhances (not replace) company specific dispatching policies such as proprietary policies for setup at specific machine groups and/or bottleneck sections of the FAB. MIVP[®] rules are distributed throughout the factory and respond dynamically in real time to variability's that occur on the FAB floor making decisions for the next set of wafers to be processed on the available resource.

Product Entry

The following diagram (Figure 2.) shows the arrival of the two products and test wafers at a constant rate of 1 lot (48 wafers) every 2 hours using the arrival *stats Generator icon* from the Extend® Discrete Event Library. Each product/device and test wafers are timed by a clock-in and clock-out routine called the *Timer icon*, also from the Discrete Event Library. This icon maintains the average cycle time over the simulated production run. The products are counted using the *Count Items icon*. The process time attributes are assigned for each step in the process flow with the *Set A(5) icon* from the Discrete Event Library. Each product/device and test wafers are sent to the router using the *Throw icon* to start the manufacturing process.

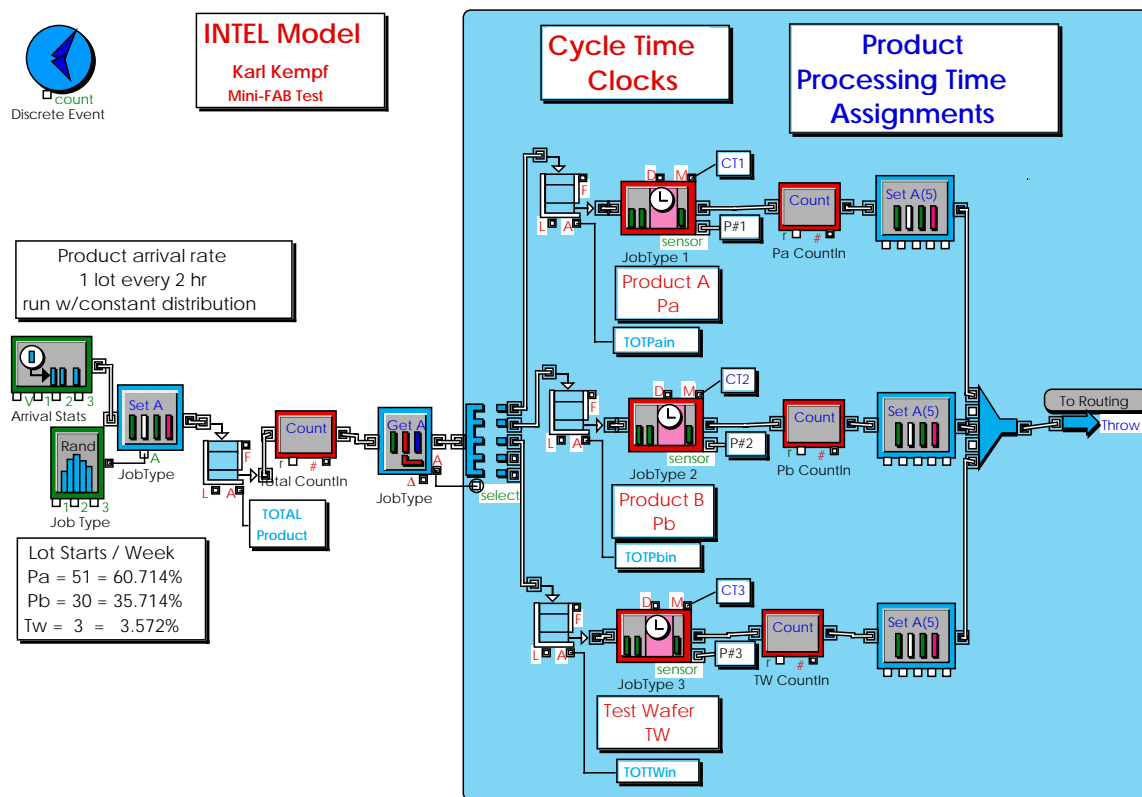


Figure 2. Extend Model – product arrivals

The Production Router (Figure 3.) for the Reentrant Process Flow

The manufacturing design team has preset the process flow of each product through its production life. This process flow plan establishes the number of steps and the machine or machine groups the product will visit through its production cycle. This sequence (routing) must be followed precisely for the production yield to be achieved. In a simulation model attributes

assigned to the product such as the process step can be used to determine where the product is to be sent next, i.e., to which machine group.

The following diagram (Figure 3) shows the routing and the reentry for each product and test wafers. The first step in the process flow is when the products and test wafers arrive from the previous diagram by *the Throw to routing icon*. The *Catch (To Routing) icon* receives the lots and begins the routing process. The reentry for the three stages allows the product to reenter the router for the next step in the process flow. The routing (or process flow) for all products and test wafers includes six steps as follows: Machine Group 1, Machine Group 2, Machine Group 3, Machine Group 2, Machine Group 1, Machine Group 3, then Exit.

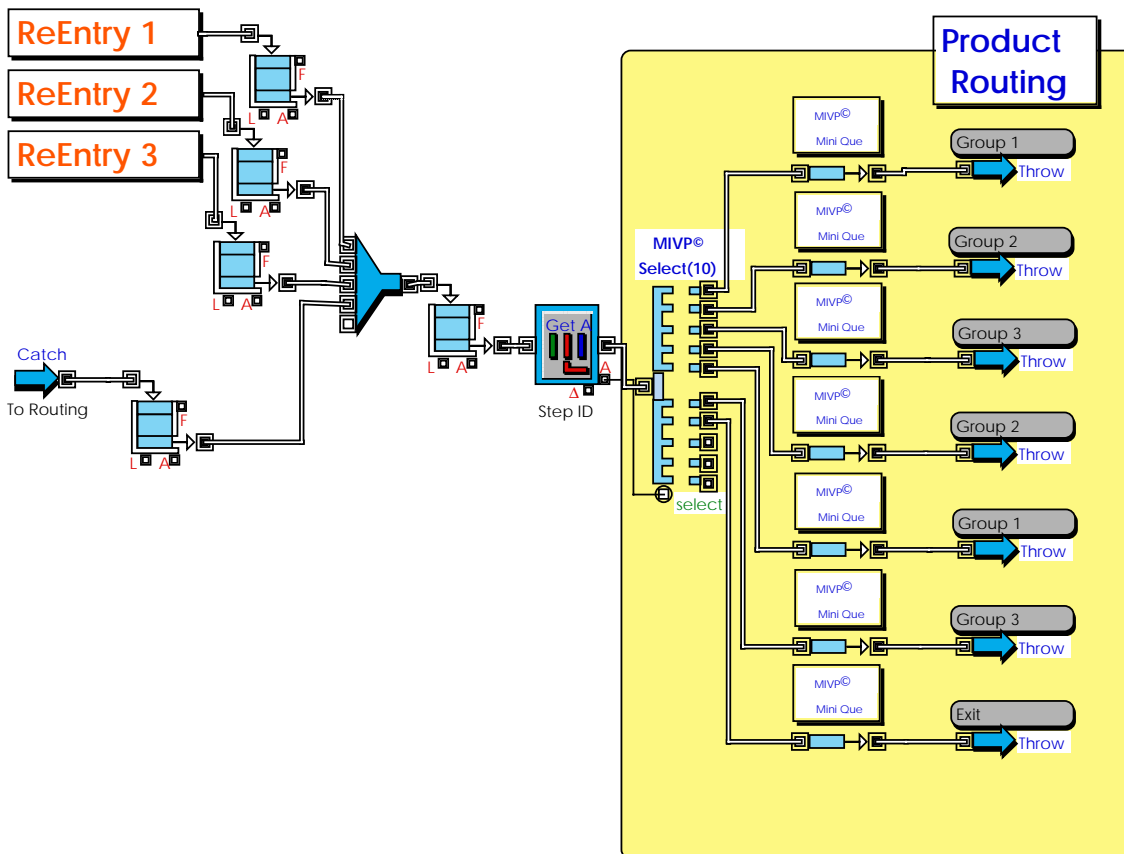


Figure 3. Product Router and Reentry

The three Machine Groups, Diffusion, Implant, and Photolithography (Figure 4.)

The following diagram shows the three machine groups, which are utilized in the process flow and the router of the previous page. The diffusion bay receives step 1 and steps 5 and requires a setup or batching of wafers in a specific manner required by the INTEL Mini-Fab Spec. (See next two pages for batching rules). Each machine group has a *queue pick selector block*, a hierarchical block that can be switched from FIFO to MIVP[®]. See pages 7, 9, and 11 for the

details for each “*Que Pick Selector*” in front of the three machine groups. After the lot has been processed it is returned to the router for the next step in the process flow (ReEntry 1, 2, 3).

The products to be batched arrive at machine group 1 for steps 1 and 5. The first *Get A icon* (get attribute) determines the step for which the products are to be batched. All products that arrive for step 1 are sent to the “Batcher for Step 1” (see below) and the products for step 2 are sent to the “Batcher for Step 2” (see next page). All step 1 batches have 7 possible combinations and step 5 batches have 4 combinations. Products A and B are used in 5 of the combinations for step 1 and 2 of the combinations in step 5. The test wafers are used in 3 of the combinations in step 1 and in 2 combinations of step 5.

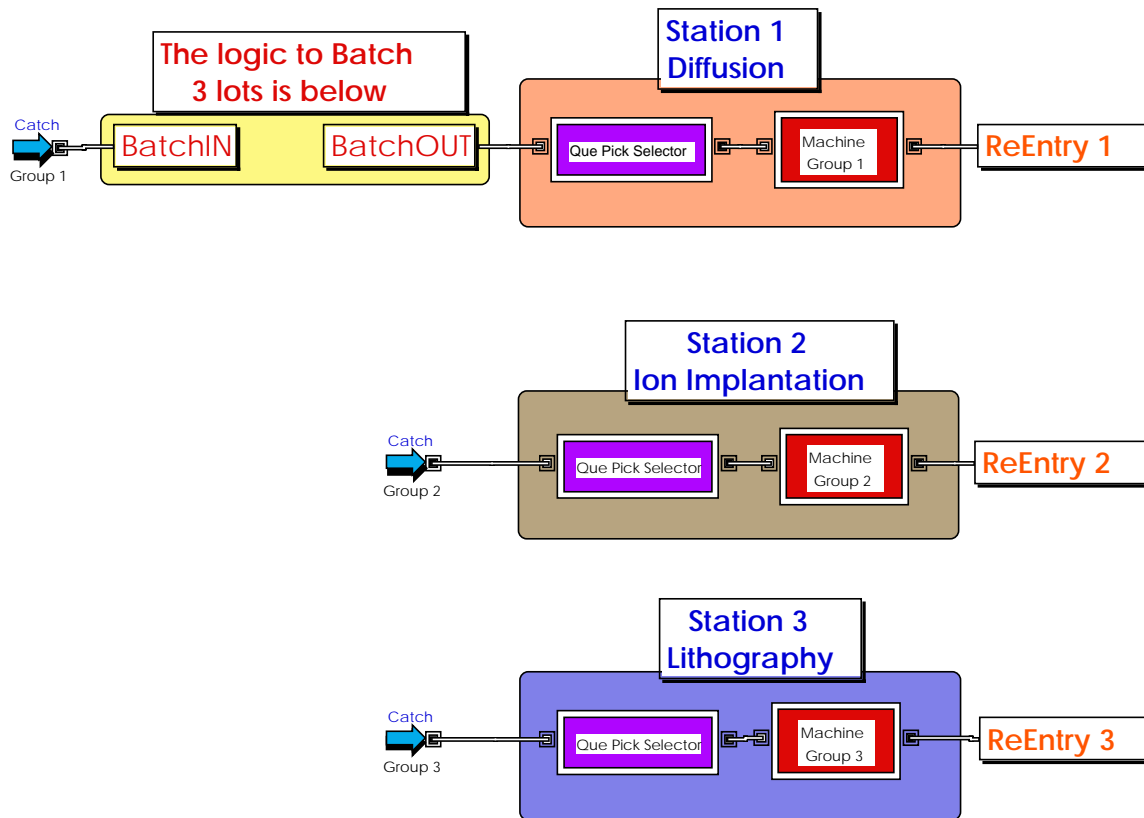


Figure 4. Machine Groups, Diffusion, Implant, and Photolithography

Company Specific Batching Rules for Diffusion Furnaces for Step 1 (Figure 5.)

The following diagram shows the rule set for the batching requirement for step 1 in the process flow. The rules are: there may be 3 lots of product Pa (PaPaPa), 3 lots of product Pb (PbPbPb), 1 lot of product Pa, 1 lot of Pb and 1 lot of test wafers TW (PaPbTW), 2 lots of product Pa and 1 lot of Pb (PaPaPb), 2 lots of product Pb and 1 lot of Pa (PbPbPa), 2 lots of product Pb and 1 lot of test wafers TW (PbPbTW), 2 lots of product Pa and 1 lot of test wafers TW (PaPaTW). The *batch icon* from the Discrete Event Library of Extend[®] allows for all three combinations of product in any desired order and quantity. The *Set A icon* (set attribute) icon sets the batch type for ordering the priority in the queue with MIVP[®] for Machine Group 1, process step 1.

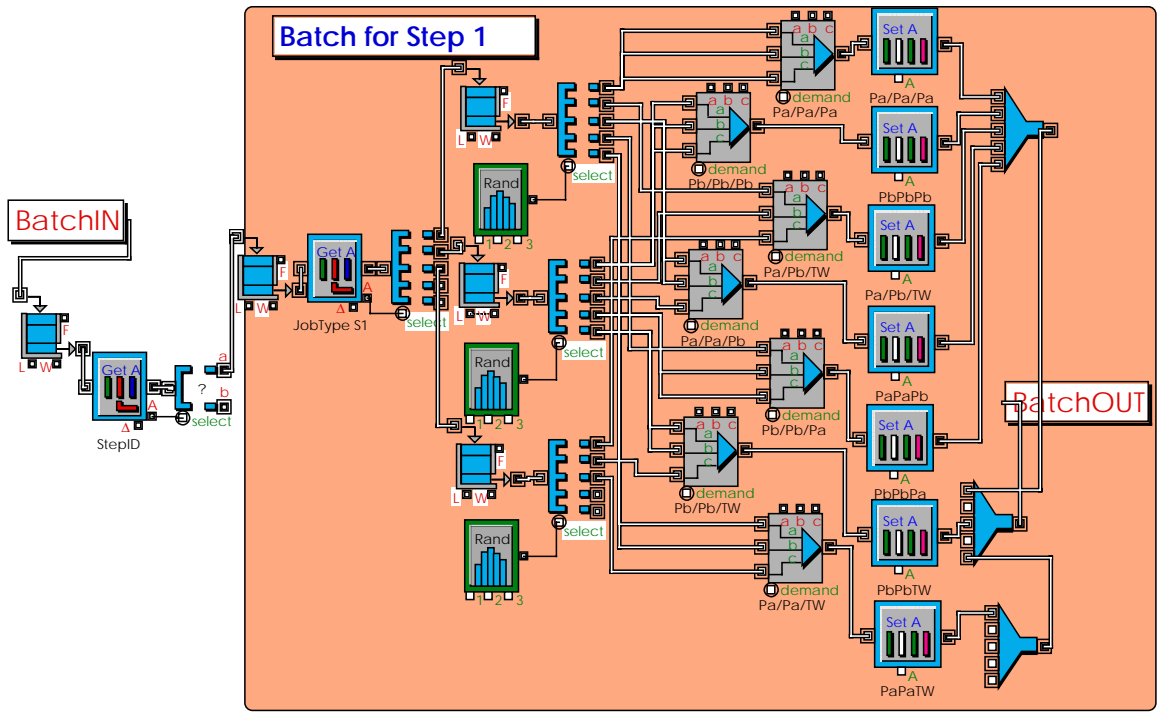


Figure 5. Company Specific Batching Rules for Diffusion Furnaces for Step 1

Company Specific Batching Rules for Diffusion Furnaces for Step 5 (Figure 6.)

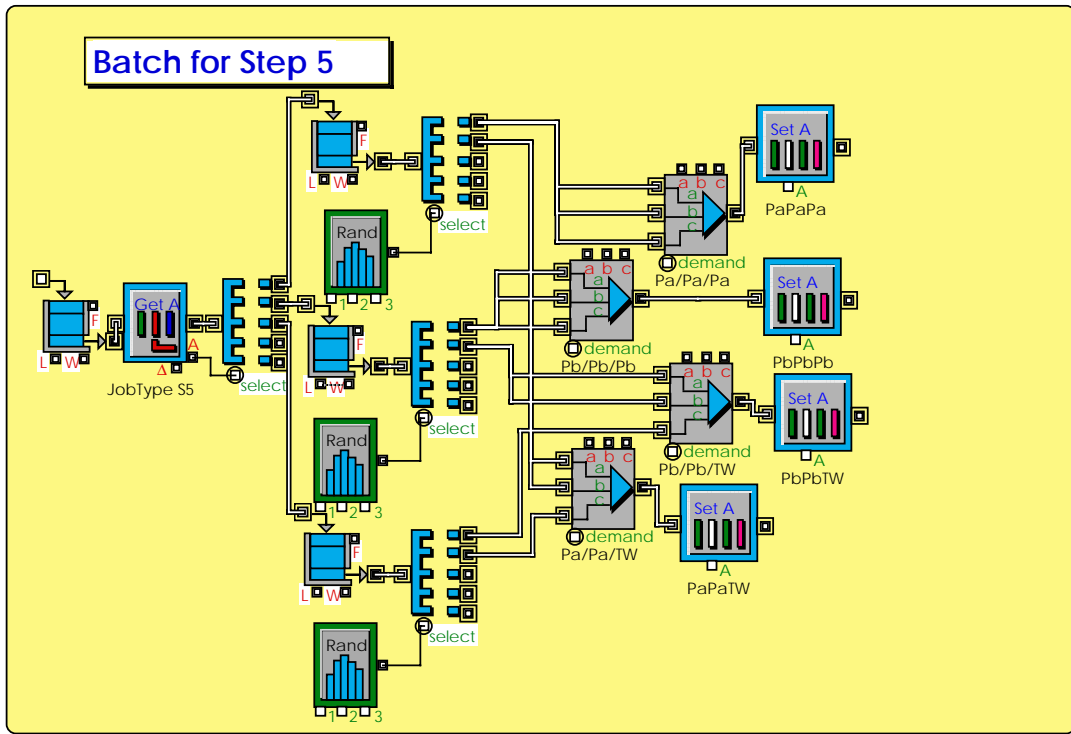


Figure 6. Company Specific Batching Rules for Diffusion Furnaces for Step 5

The above diagram (Figure 6.) shows the rule set for the batching requirement for step 5 in the process flow. The rules are: there may be 3 lots of product Pa (PaPaPa), 3 lots of product Pb (PbPbPb), 2 lots of product Pb and 1 lot of test wafers TW (PbPbTW) and 2 lots of product Pa and 1 lot of test wafers TW (PaPaTW),. The *batch icon* from the Discrete Event Library of Extend[®] allows the assembly of three combinations of product in any desired order and quantity. The *Set A icon* (set attribute) sets the batch type for ordering the priority in the queue with MIVP[®] for the reentry of Machine Group 1, process step 5.

Queue Pick Selector (FIFO or MIVP[®]) for Machine Group C1 – Diffusion Furnaces

The following diagram (Figure 7.) shows the queue pick selector for steps 1 and 5 in the process flow at machine group 1. Several custom icons produced for the semiconductor industry by ACADZ inc. are used in this hierarchical block. The key icon is the *MIVP[®] 20 Que Pick*, which can be switched from the MIVP[®] rules to FIFO. When the switch is set to FIFO, the first product batch that arrives is the first to be processed on the next available machine. FIFO does not differentiate for batched products in step 1 or step 5. MIVP[®] on the other hand makes a choice using its rule structure, e.g., if machine Me (step 6) is down for maintenance, MIVP[®] will select a batched product for machine group C2 (step 2) if one is available. The rule here is to “correlate the present available process time with the next process step availability”. This is one of the many rules within MIVP[®].

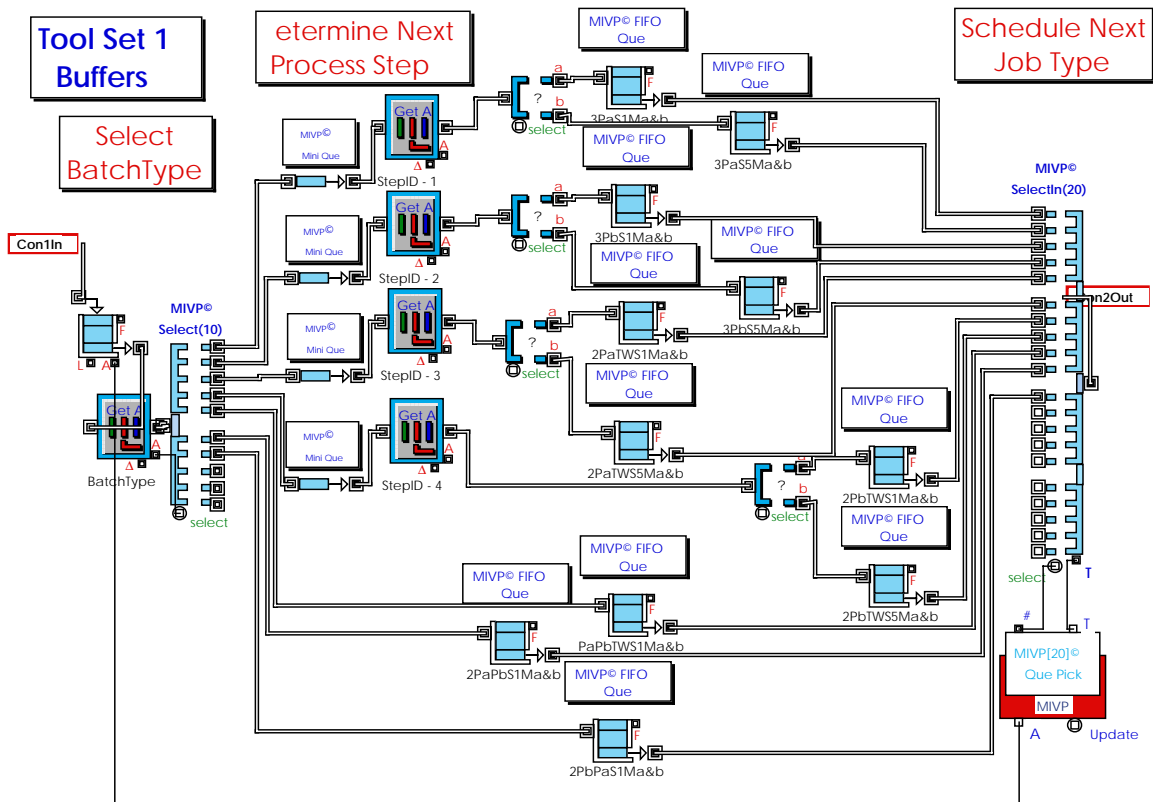


Figure 7. Queue Pick Selector (FIFO or MIVP[®]) for Machine Group C1

The switch is set to FIFO for the baseline data collection. Once the model has been run and the data has been collected for FIFO, the MIVP[®] schedule policies are switched on and the model is run again for the same production time. The average cycle time results from MIVP[®] are then compared to FIFO.

Machine Group C1 – Diffusion Furnaces with PID and H-Infinity Controllers

The diagram below (Figure 8.) represents machine group C1, the two machines Ma and Mb, diffusion furnaces. The batched lots arrive and are processed on the next available machine (furnace). The furnace is taken down for emergency maintenance based on prescribed alarm/abort conditions. A typical concern with diffusion processes is the drift of the thermocouple measurements with every operation. Its net effect is that the actual processing temperature is slowly drifting away from the desired one, specified by the recipe. In order to keep the product within acceptable limits, alarm/abort conditions can be specified indirectly (based on required average power) or directly (using metrology results after the step). For simplicity, in our study we only consider the second case. We also emulate the drift with a small increment in the processing temperature every time the process is operated. To obtain the statistics of emergency maintenance for this process we use a MATLAB[®]-based simulator that was developed in the context of controller design for diffusion/CVD furnaces¹⁸. The furnace temperature model is obtained using system identification techniques on actual furnace data and provides a fairly faithful representation

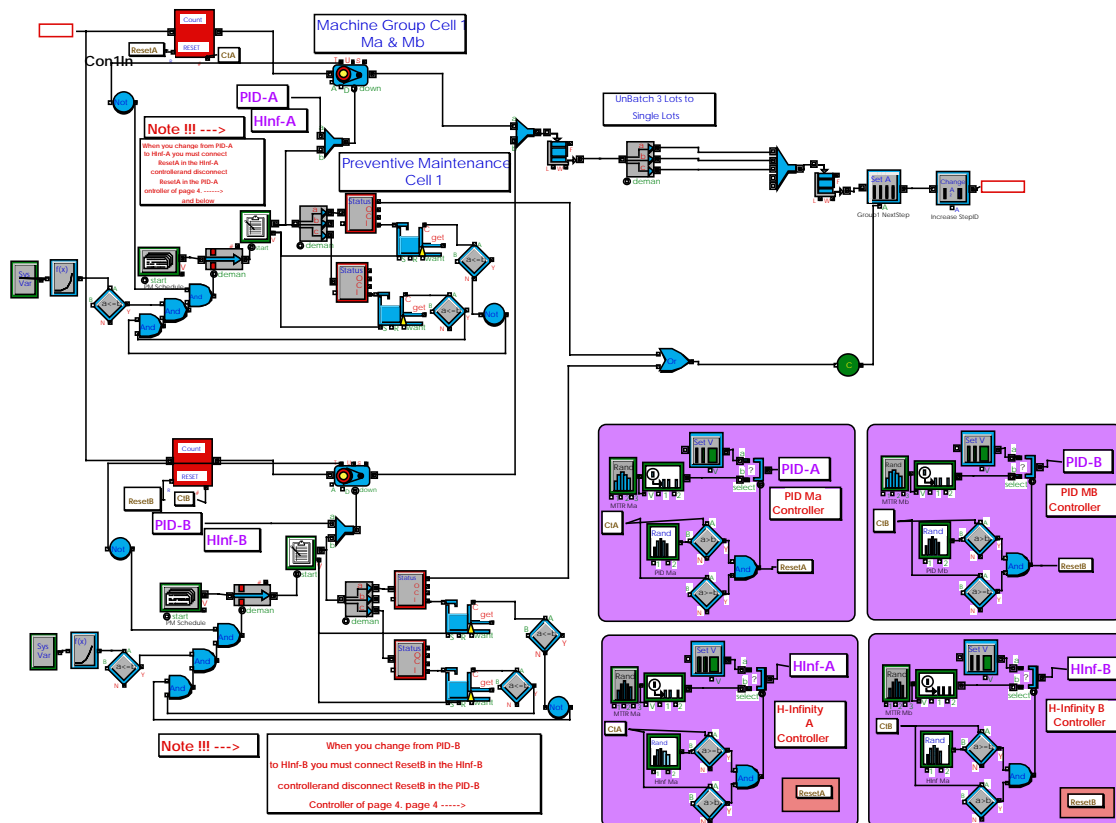


Figure 8. Machine Group C1 – Diffusion Furnaces with PID and H-Infinity Controllers

of the furnace behavior. The simulated temperature is then translated into deposition thickness using a standard Deal-Grove oxidation model. From a high-level scheduling perspective, the variable of interest is the statistics of the emergency maintenance time. Clearly, its mean value depends on the rate of the thermocouple drift. However, its variance depends on the real-time properties of the process and the associated low-level controller. To compute the required statistics, several low-level simulations are performed and the results are entered in the Extend[®] simulator. Finally, to investigate the effect of the maintenance time variance, we compute the statistics for two controllers, a (detuned) PID Controller and a (high performance) H-Infinity Controller. The diagram shows that the PID controller is being tested.

Queue Pick Selector (FIFO or MIVP[®]) for Machine Group C2 – Implant

The following diagram (Figure 9.) shows the queue pick selector for step 2 and step 4 in the process flow for the Implant Machines Mc and Md. The rules are switched to FIFO for the baseline data collection. Once the model has been run and the data has been collected for FIFO, the MIVP[®] schedule policies are switched on and the model is run again for the same production time. The average cycle time results from MIVP[®] are then compared to FIFO.

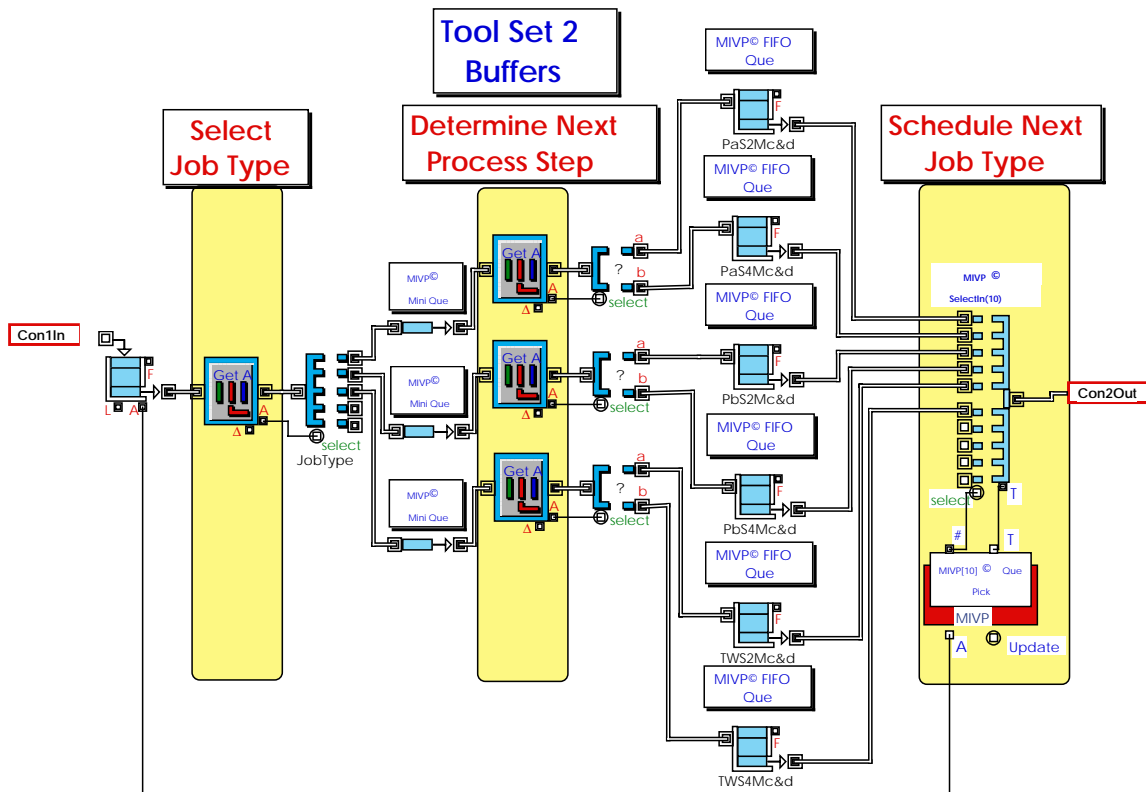


Figure 9. Queue Pick Selector (FIFO or MIVP[®]) for Machine Group C2 – Implant

Machine Group C2 – Implant with Historical Emergency Maintenance

The diagram below (Figure 10.) represents the two machines Mc and Md, for Implant. The lot will arrive and be processed on the next available machine. The Implant Machines will be taken down for emergency maintenance according to historical data for mean time before failure MTBR and mean time to repair MTTR. The diagram also shows preventive maintenance with a specific rule set for PM.

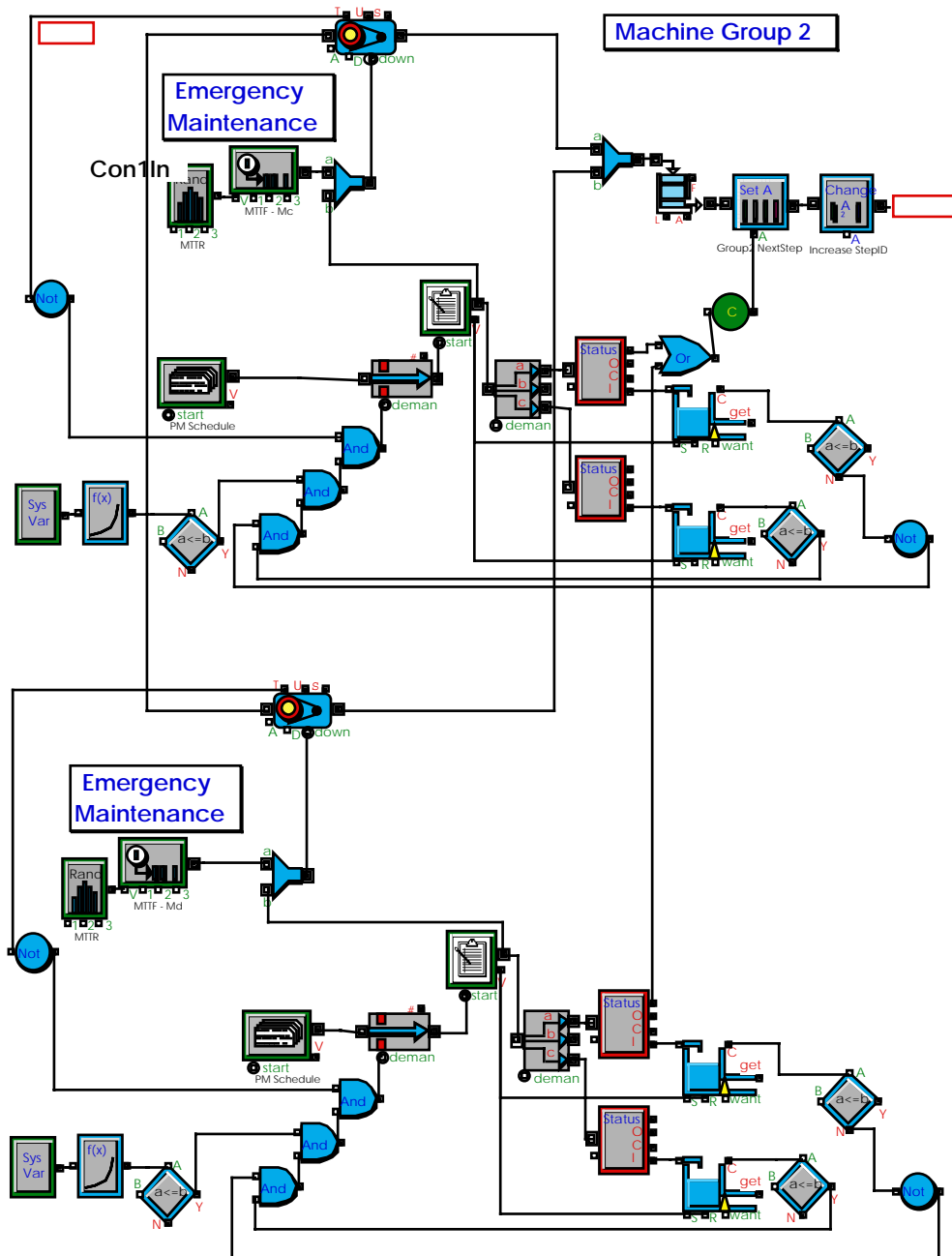


Figure 10. Machine Group C2 – Implant with Historical Emergency Maintenance

Queue Pick Selector (FIFO or MIVP[®]) for Machine Group C3 – Photolithography

The following diagram (Figure 11.) shows the queue pick selector for step 3 and step 6 in the process flow for the Photolithography Machine Me. The rules are switched to FIFO for the baseline data collection. Once the model has been run and the data has been collected for FIFO, the MIVP[®] schedule policies are switched on and the model is run again for the same production time. The average cycle time results from MIVP[®] are then compared to FIFO.

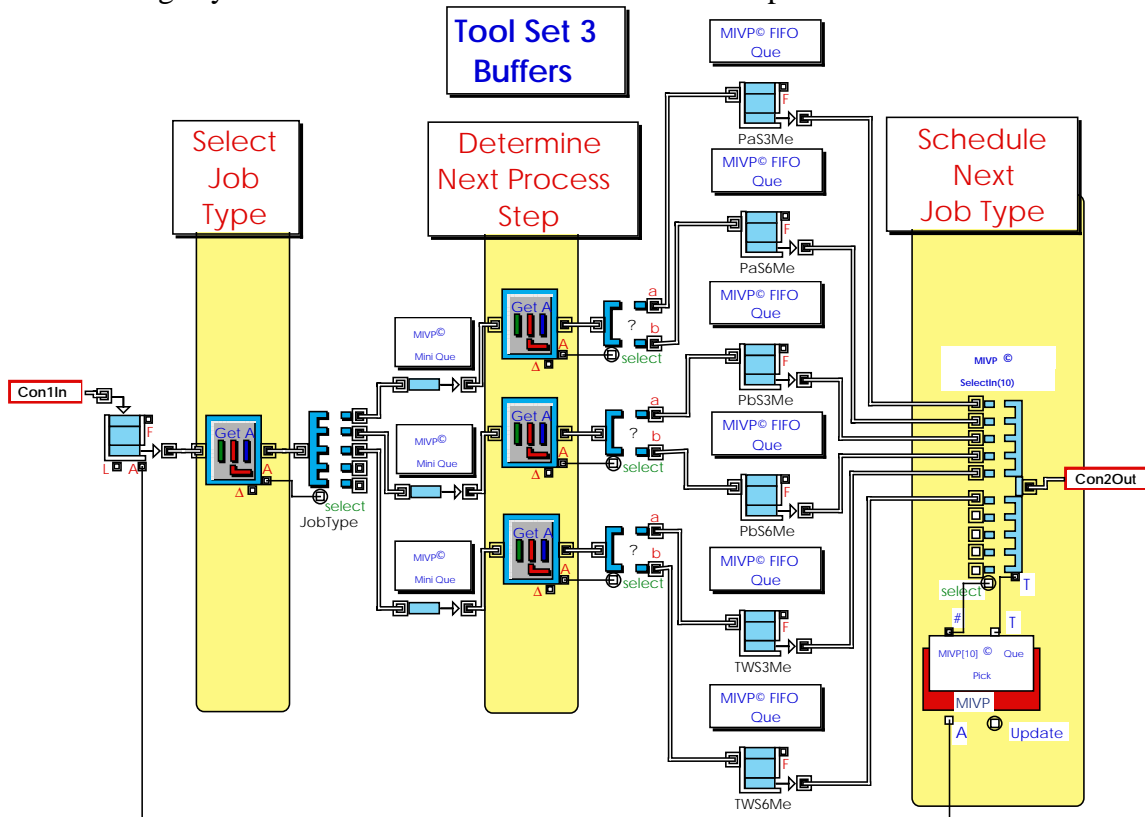


Figure 11. Queue Pick Selector (FIFO or MIVP[®]) for Machine Group C3

Machine Group C3 – Photolithography with Setups and Preventive Maintenance

The diagram below (Figure 12.) represents the Photolithography Bay machine Me, the Photo Stepper. The lot arrives and is processed on the machine. This machine has a set of rules for setup because the reticle requires changing for each different product as well as each different layer. The Photo Stepper Machine will be taken down for emergency maintenance according to historical data for MTBR and MTTR. The diagram also shows preventive maintenance with a specific rule set for PM.

The diagram below (Figure 13.) shows the icons for collecting statistics during the production run. Work-In-Progress (WIP), average cycle time and product exit information is displayed in numerical form as well as graphically. Queue statistics of arrivals, departures, size of queue, and utilization are important for playing “What If” scenarios. The mean and variance of each machine is also displayed numerically and graphically.

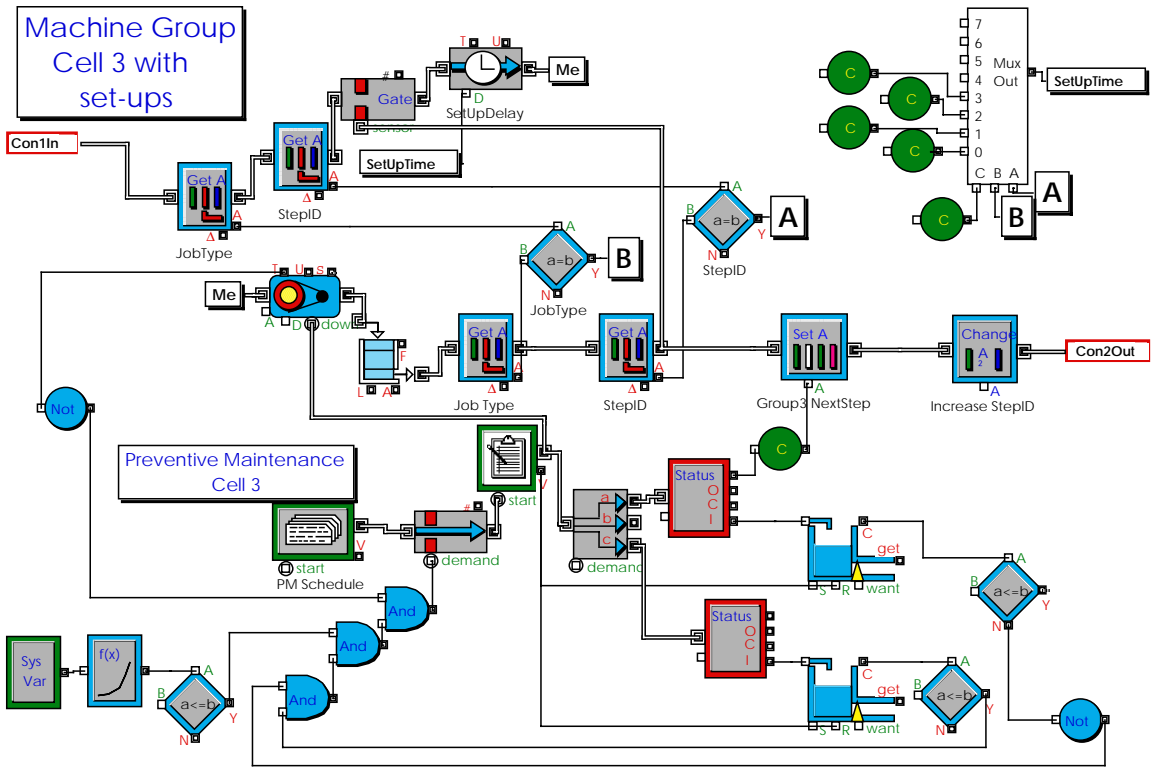


Figure 12. Queue Pick Selector (FIFO or MIVP[®]) for Machine Group C3

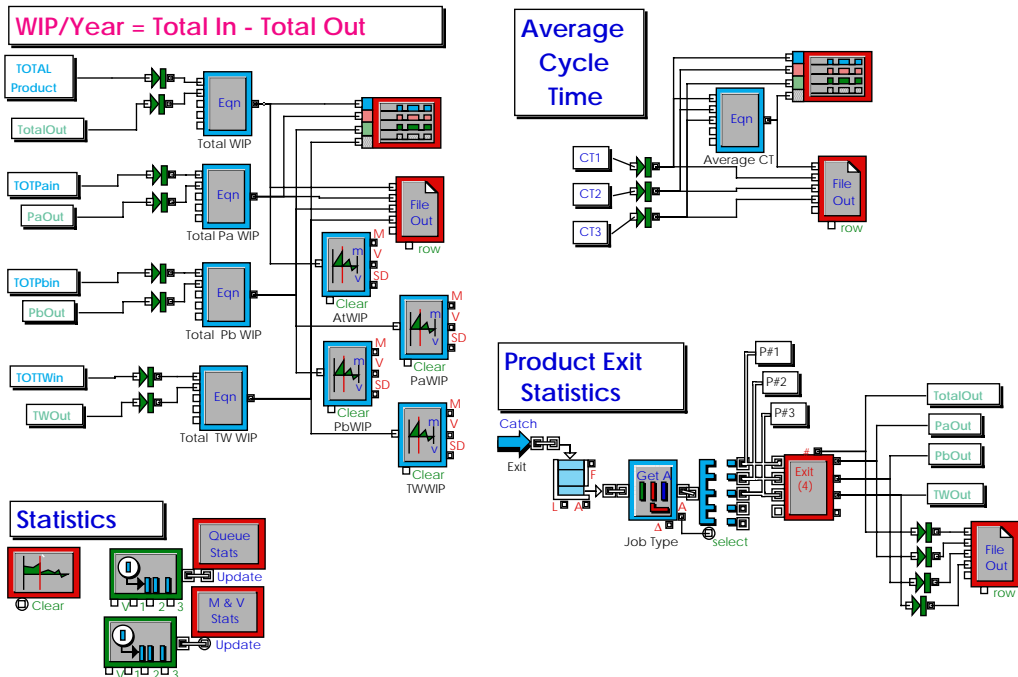


Figure 13. Data Collection for Production, Cycle Time, Work-in-Progress and Model Statistics

Results

The following tables summarize the results of our simulation study and demonstrate the effects of high-level scheduling policies and low-level controller variance on the production statistics.

Table 1. Kempf Mini-FAB Model Results, no setup's and 1 lot per 120 minutes

	Product Averages	Product Pa	Product Pb	Product TW
PID Mean Cycle Time, FIFO	4134.0±88.3	4155.1±90.8	4858.7±85.3	3388.1±96.0
H[∞] Mean Cycle Time, FIFO	3462.4±23.5	3499.4±14.6	4194.1±25.3	2693.5±60.4
PID Mean Cycle Time, MIVP[®]	3899.3±62.6	4176.7±75.5	4605.4±63.4	2915.7±63.3
H[∞] Mean Cycle Time, MIVP[®]	3373.8±22.3	3519.4±16.0	4082.1±30.9	2520.0±45.8
Raw Processing Time¹	1277.915±0.90	1277.915±0.9	1277.915±0.90	1277.915±0.90
TQT², PID FIFO	2856.1235	2877.2493	3580.8557	2110.2656
TQT, H[∞] FIFO	2184.5004	2221.5628	2916.255	1415.6834
TQT, PID MIVP[®]	2621.3977	2898.8603	3327.5275	1637.8051
TQT, H[∞] MIVP[®]	2095.9532	2241.5301	2804.1914	1242.1381
PID Mean WIP³, FIFO	39.20±2.18	23.23±1.73	15.03±1.50	0.933±0.373
H[∞] Mean WIP, FIFO	29.83±1.60	17.40±1.19	11.56±1.17	0.866±0.343
PID Mean WIP, MIVP[®]	36.40±1.56	22.86±1.76	12.36±1.54	1.166±0.671
H[∞] WIP, MIVP[®]	29.16±1.23	16.66±0.805	11.90±0.897	0.600±0.219

Comparison among the Mean Cycle Time for different strategies

Table 2. Product Average no setup's and 1 lot per 120 minutes

		External Policy (Outer loop)	
		FIFO	MIVP
Furnace Controller (Inner loop)	PID	1	0.9432
	H[∞]	0.8375	0.8161

Table 3. Product Pa, no setup's and 1 lot per 120 minutes

		External Policy (Outer loop)	
		FIFO	MIVP
Furnace Controller (Inner loop)	PID	1	1.0052
	H[∞]	0.8421	0.8470

Table 4. Product Pb, no setup's and 1 lot per 120 minutes

		External Policy (Outer loop)	
		FIFO	MIVP
Furnace Controller (Inner loop)	PID	1	0.9478
	H[∞]	0.8632	0.8401

Table 5. Product TW, no setup's and 1 lot per 120 minutes

		External Policy (Outer loop)	
		FIFO	MIVP
Furnace Controller (Inner loop)	PID	1	0.8605
	H[∞]	0.7949	0.7437

Acknowledgment

¹ Summation of all processing time for each step plus the time needed for batching.

² Total Queuing Time.

³ Work In Progress.

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** MIVP[®] and MIVP[®] 1-Step Ahead are registered trademarks of ACADZ, inc.

*** Kempf model specification is provided by Dr. Karl Kempf, Intel Corporation.

Bibliography

1. J. D. C. Little, "A Proof of the Queueing Formula: $L=IW$," *Operations Research*, Vol. 9, 1961, pp. 383-387.
2. Leonard Kleinrock, *Queueing Systems*, Vol. 1, John Wiley & Sons, New York, NY, 1975.
3. S. Li, T. Tang, and D.W. Collins, "Minimum Inventory Variability Schedule with Applications in Semiconductor Fabrication," *IEEE Transaction on Semiconductor Manufacturing*, Vol. 9, No. 1, February 1996, pp. 145-149.
4. El Adl, A.A. Rodriguez, and K.S. Tsakalis, "Modeling and Control of Re-entrant Semiconductor Manufacturing Lines: A Hierarchical Approach," *Proceedings of the 1996 Conference on Decision and Control*, Kobe, Japan.
5. El Adl, J.J. Flores, M. Kawski, A.A. Rodriguez, K.S. Tsakalis, "Hierarchical Modeling and Control of Re-entrant Semiconductor Fabrication Lines," *Proceedings of the 1997 American Control Conference*, Albuquerque, NM, Invited Session.
6. K. Kempf, "Detailed Description of Multiple Product Re-entrant Semiconductor Manufacturing System Example," Prepared report, Intel Corporation, Technology, and Manufacturing Group, August, 1994.
7. T.S. Cale, P.E. Crouch, L. Song, and K.S. Tsakalis, "Optimal Control for LPCVD," *Proc. Symposium on Process Control, Diagnostic and Modeling in Semiconductor Manufacturing*, The Electrochemical Society, Vol. 95-2, 97--107, Reno, May 1995.
8. D.W. Collins, K. Williams, and F.C. Hoppensteadt, "Implementation of Minimum Inventory Variability Scheduling 1-Step Ahead Policy in a Large Semiconductor Manufacturing Facility," *6th Annual IEEE International Conference on Emerging Technologies and Factory Automation*, UCLA, Los Angeles, Sept 9-12, 1997.
9. D.W. Collins and F.C. Hoppensteadt, "Investigation of Minimum Inventory Variability Scheduling Policies in a Large Semiconductor Manufacturing Facility," *1997 American Control Conference*, Albuquerque, New Mexico, June 4-6, 1997.
10. D.W. Collins and B.G. Zaslavsky, "A Numerically Effective Optimization Technique for Scheduling Time Varying Production Flows in Semiconductor Manufacturing," *INFORMS 1996 Conference*, Atlanta Georgia, November 3-6, 1996.
11. J.J. Flores-Godoy, Y. Wang, D.W. Collins, F.C. Hoppensteadt, and K. Tsakalis, "Intel Mini-FAB Simulation Model comparing machine scheduling policies of FIFO with MIVP[®] with constant release policy and using a PID controller and H[∞] controller for the diffusion bay for a priori maintenance." Presented at the SSERC Seminar of Multiscale Integration of Manufacturing and Assembly Processes, October 17, 1997, ASU.
12. F.C. Hoppensteadt, *Analysis and Simulation of Chaotic Systems*, Springer-Verlag, New York, 1993.
13. K.S. Jun, D.E. Rivera, K.S. Tsakalis, H.M. Liaw, E. Hall, and C. Stein, "PID Optimization for Temperature Control of Epitaxial Growth," *Proc. ECS Conference*, 373--374, Montreal, Feb. 1997.
14. K. Kempf, Detailed description of a two-product, six-step five-machine re-entrant semiconductor manufacturing system, prepared report, Intel Corporation, Technology & Manufacturing Group, August, 1994.
15. J.J. Kristoff, L.J. Song, K.S. Tsakalis, and T.S. Cale, "Optimally Controlled Programmed Rate Deposition of Tungsten," *VLSI Multilevel Interconnect Conference*, Santa Clara, CA, June 1997
16. N. Srivatsan, and K. Kempf, "A linear programming model of a re-entrant system, prepared notes," Intel Corporation, Technology & Manufacturing Group, July, 1994.
17. K.D. Stoddard, P.E. Crouch, M. Kozicki, and K.S. Tsakalis, "Application of Feed-Forward and Adaptive Feedback Control to Semiconductor Device Manufacturing," *Proc. American Control Conference*, 892--896, Baltimore, 1994.
18. M. Tucker, E. Valdez, K. Tsakalis, M. Warren and K. Stoddard, "Improving Vertical Furnace Performance Using Model-Based Temperature Control," *AEC/APC Symposium X*, Vail CO, Oct. 98.

19. K.S. Tsakalis, J.J. Flores-Godoy, and A. A. Rodriguez, "Hierarchical Modeling and Control of Re-Entrant Semiconductor Fabrication Lines: A Mini-Fab Benchmark," *Proc. 6th IEEE Int. Conference on Emerging Technologies and Factory Automation*, Los Angeles, Sept. 1997, pp. 508-513.
20. K.S. Tsakalis, and K.D. Stoddard, "Integrated Identification and Control for Diffusion/CVD Furnaces," *Proc. 6th IEEE Int. Conference on Emerging Technologies and Factory Automation*, Los Angeles, Sept. 1997, pp. 514-519.

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