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Modular Integrated Stackable Layer (MISL): An Academic-Public Sector Partnership for Rapid Prototyping and Development

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Modular Integrated Stackable Layers (MISL): An Academic-Public Sector Partnership for Rapid Prototyping and Development

Abstract

The rapid product development process continues to increase its demands on hardware prototyping tools. These tools need to create prototypes with higher levels of functional integration necessary to accommodate a diverse selection of embedded intelligence, sensors, actuators, communications and data storage technologies. In addition, the turn-around time from prototype to commercialized product continues to decrease so that companies can be first to market, thus gaining important market share. Although there are a number of hardware development tools available, none of these fully meets the demanding requirements of the aerospace, automotive, communications, medical, petrochemical industries[1.] Based on a number of successful applied research and capstone design projects, the Controls and Data Handling Branch at National Aeronautics and Space Administration - Johnson Space Center (NASA-JSC) recently formed a development partnership for its unique Modular Integrated Stackable Layer (MISL) architecture with the Electronic Systems Engineering Technology Program (ESET) at Texas A&M University. The MISL architecture encompasses a series of layers (printed circuit boards) that can be quickly "stacked" into a small form factor footprint that provides a wide range of technologies. Developers can quickly configure an application-specific configuration by selecting from multiple options for power, microcontroller, communications, sensors and other signal conditioning circuitry. The ESET Program has three primary responsibilities to the newly formed partnership: 1) New layer design, 2) Educational course and laboratory material development, 3) Establishment of an open development community environment. This paper provides an overview of the MISL partnership, the educational and research activities that have been successfully conducted to date, the lessons learned, and the move forward plans for the space qualified rack-and-stack hardware development platform.

Introduction

The rapid product development demands on hardware prototyping tools continue to increase. These tools need to accommodate a diverse selection of embedded intelligence, sensors, actuators, communications and data storage technologies to create fully functional prototypes quickly and with higher levels of integration. In addition, the turn-around time from prototype to commercialized product continues to decrease so that companies can gain important market share by being first to market. Although there are a number of hardware development tools available such as Arduino, Raspberry Pi, etc., none of these is fully capable of supporting the rigorous demands of harsh operational environments found in aerospace, automotive, oil & gas, medical, or communications systems prototyping.

In addition, educational programs need to have similar resources that support a flexible and reconfigurable toolset for undergraduate education from entry-level courses at the sophomore level to final Capstone/Senior Design projects[2]. There is significant value in a resource such as this that can be configured to support not only embedded systems software courses, but to have the ability to be used in other courses such as instrumentation, control systems, and communications. Bringing technologies that can meet the demanding needs of industry into the

educational classroom/laboratory can also provide new opportunities for academia-industry collaboration and development projects.

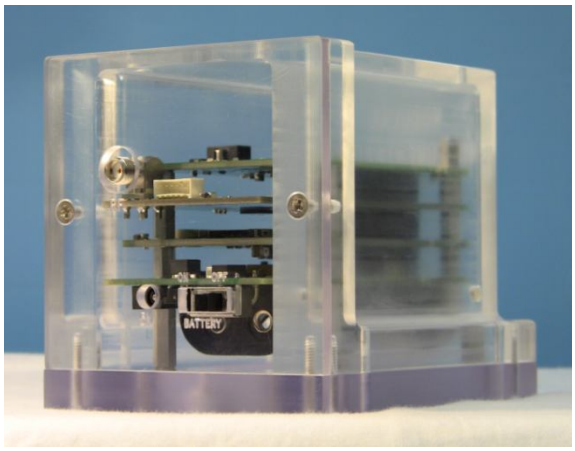

Figure 1. MISL Demo Unit.

Based on a number of successful applied research and capstone design projects, the Controls and Data Handling Branch at National Aeronautics and Space Administration - Johnson Space Center (NASA-JSC) recently formed a development partnership for its unique Modular Integrated Stackable Layer (MISL) architecture with the Electronic Systems Engineering Technology (ESET) Program at Texas A&M University. NASA has emphasized the opportunity to build bridges with academia through partnership development activities such as this[3]. The MISL architecture depicted in Figure 1 encompasses a series of layers (printed circuit boards) that can be quickly "stacked" into a small form factor footprint that provides a wide range of capabilities. Developers can quickly assemble an application-specific configuration by selecting from multiple MISL layers for power, microcontroller, communications, sensors and other signal conditioning circuitry. The ESET Program has three primary responsibilities to the newly formed partnership: 1) New layer design, 2) Educational course and laboratory material development, 3) Establishment of an open development community environment. This paper provides an overview of the MISL partnership, the educational and research activities that have been successfully conducted to date, the lessons learned, and the move forward plans for the space qualified rack-and-stack hardware development platform.

MISL Concept of Operation

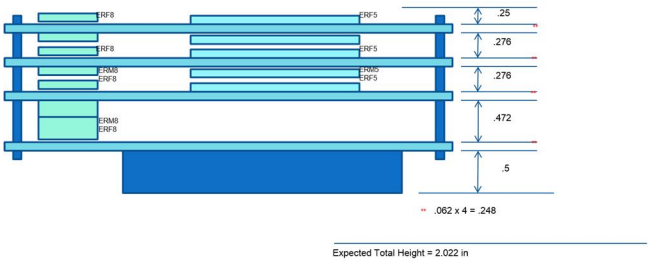

Figure 2. MISL Architecture.

As shown in Figure 2, the NASA/MISL partnership with the Texas A&M ESET Program is based on the concept of co-development of a series of small form factor functional layers that have the ability to stacked together to form a complete and user-definable development system. The system architecture includes layers that provide power, embedded intelligence, communications, sensors, and actuators[4]. Each layer is individually designed and developed to conform to the NASA-managed MISL bus architecture and can then undergo space-qualification testing if selected by NASA. As the number of different layers are developed, the embedded systems designer will be able to choose between a range of different options in each of these categories to implement the specific system needed for the application. For example, a particular application might require battery power, an energy efficient microcontroller, 802.11 wireless communications, an accelerometer and motor controller. Using the MISL architecture, a

hardware system is assembled in a matter of minutes to support this development need, because all modules adhere to both the power and data bus specifications established by NASA. The concept of operation also includes the ability to quickly "collapse" the design into a single printed circuit board so that significant cost savings can be realized should the newly developed system require large quantity production.

The partnership's overall goal for the MISL architecture is to provide an embedded instrumentation and control system that is

- Modular
- Scalable
  - Multiple board stacks to meet specific design requirements
  - Standards-based to allow for PCB to grow in size when necessary
- Reusable
- Flexible
- Quick to market
- Industry Standard Interfaces
- Harsh Environment capable
  - Temperature
  - Vibration
  - Radiation tolerant

Potential uses of the MISL architecture include:

- Remote autonomous data acquisition
- Distributed instrumentation
- System control
- Wired/wireless communications

Hazardous application areas include:

- Aerospace
- Automotive
- Communications
- Medical
- Oil & Gas

MISL Layers

Currently, the partnership has developed a series of MISL layers that can provide rapidly configurable hardware solutions across a wide range of applications. Each of the layers is intended to meet one or more of the typical requirements of an embedded system. The design files for those that have been developed by NASA-JSC have been transferred to the ESET Program. A number of these layers have been procured by the ESET Program and are being used in both educational and development applications. The ESET Program through its Capstone Design and applied research projects is also developing new MISL layers as part of the project functional requirements. In so doing, the partnership is leveraging the layers already developed while adding to the repertoire of hardware functions that can be selected to satisfy the needs of future projects. When appropriate, NASA submits a new layer to space qualification

testing. Both NASA and ESET can also continue to refine any of the current designs to expand capability, reduce cost, or improve performance. High level descriptions for a range of layers currently available are provided.

Power Layers. Two different MISL power layers are currently available. These are

1) 28VDC Input Power Layer, and
2) Battery (Three 1.5V AA Batteries/5VDC Input Power Layer.

Figure 3. 28VDC Power Layer.

The 28VDC layer shown in Figure 3 supports the power available on the International Space Station and other NASA space vehicles. The second power layer can operate from three AA batteries or be powered by a 5VDC wall wart. These options support development/test of new embedded systems in the laboratory with the ability to transfer the system to space power (28VDC) by just changing out the power module.

Intelligence Layers. Three embedded intelligence microcontroller) layers are available. These are

1) MSP430 microcontroller,
2) Concerto (F28M36x) microcontroller (ARM and DSP), and
3) RM48 microcontroller shown in Figure 4.

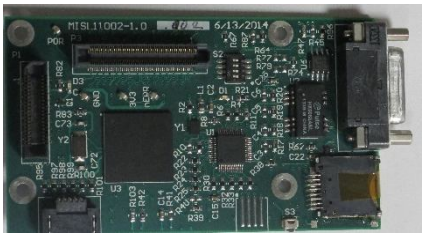

Figure 4. RM48 Intelligence Layer.

These three selections provide a series of options that support applications ranging from ultra-low power to system on a board capability. Other options currently being considered include a Microchip PIC32 layer. The capability to support Real Time Operating System (RTOS) development is also available using the MISL intelligent layers.

Communications. A wide range of wired/wireless communications layers are available. Wired interfaces include

1) UART serial and
2) 802.3 Ethernet.

The wireless interfaces presently available include

1) 802.11b/g/n Board shown in Figure 5,
2) Zigbee Mesh Network Board,
3) 802.15.4A Wireless Personal Area Network Board, and
4) ISA 100.11 Wireless Board.

Figure 5. 802.11 Communications Layer.

A Capstone Design project currently underway will expand this category of layers by adding a cellular modem layer capable of both voice and data communications.

Sensor/Actuator. A number of layers have been developed for this category including

1) Multi-sensor demo board shown in Figure 6,
2) 4-20mA sensor interface board,

Figure 6. Multi-Sensor Layer.

3) Charge amp board for Tri-axel Accelerometer,
4) Analog Voltage Board,
5) High Voltage Instrument Interface Board,
6) Solenoid Value Interface Board, and
7) High-Speed DAQ Board.

Analog System Environment (ASE). The ASE (Pronounced "ACE") Board depicted in Figure 7 is a new addition to the MISL architecture. It is intended to be used primarily for educational purposes, but also demonstrates the flexibility of the NASA-defined power and data buses to support larger form-factor Printed Circuit Boards. This layer is much larger than the typical MISL layers and includes a number of modules that can be used in an educational laboratory environment. Within the ESET Program this new MISL layer is scheduled to be used to support three embedded software development courses/laboratories and the RTOS technical elective course. The MISL MSP430 intelligence layer can be plugged into the ASE layer (as shown in bottom left corner of figure) to form a complete embedded system. Future Capstone teams will be able to take advantage of the breadth of technologies provided by the ASE Board to rapidly assemble their development environment to support initial software design and testing. The ASE layer includes:

Figure 7. New MISL-ASE Board.

GPIO – Outputs
- 5 LEDs with 4 colors (blue, red, yellow, green)
- 1 Tri-color LED (blue,red,green)
- Breathing LED
- 8 7-segment displays
- TFT LCD Display with touch screen
- 1602 LCD Display
- Buzzer

GPIO - Inputs
- 4x4 Matrix Keypad
- 4 Switches

A/D Conversion
- A/D - Analog Voltage Simulation with Potentiometer
- A/D - External Signal Conditioning
- A/D - Battery Life Measurement
- A/D - 3-Axis Accelerometer
- One 16-bit Resolution (8-Channel) Serial ADC Converter (SAR)

D/A Conversion
- D/A - Signal Generation (Sine, triangle, square, etc.)
- D/A - LED Brightness

SPI
- Ethernet
- Wi-Fi
- uSD Card
- Flash Memory

UART
- USB
- RS-232/485
- Bluetooth
- Zigbee

I2C
- DAC
- EEPROM

One-Wire Communication
- Temperature Sensor

Motor Control & Relay
- Stepper Motor
- DC Motor

Rechargeable Backup Battery

Standard JTAG Interface

Current Status/Future Plans

The opportunity to design, develop, document, and deliver new MISL layers as part of the ESET Capstone Design sequence continues to expand[5]. Using the design and development resources of ESET Product Innovation Cellar[6], the project performed during the Spring/Fall 2014 semesters produced a new 10-layer RM48-based intelligence layer shown in Figure 8. This new intelligence layer was then used to develop a new integrated wireless monitoring, control and remote display robotic system that was integrated into the ESET Articulated Suspension Evaluation Platform (ASEP) ground robot. The project team members were not only highly motivated by working with NASA-JSC engineers, the interaction allowed them to appreciate the design process and methodologies used by a federal agency. All aspects of their project were reviewed and improved through close interaction with NASA hardware design engineers. In addition to successfully completing their Capstone project, the team was able to add value to their experience through several other related activities. These included

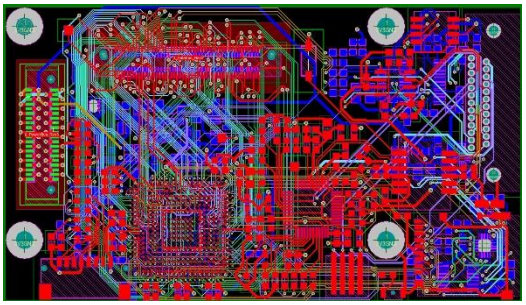

Figure 8. RM 48 Layer PCB Layout.

1. *First Place* – Student Paper at 2014 ASEE Gulf-Southwest Conference[7]
2. *Frist Place* – Industry Choice Award, 2014 Texas A&M Look College of Engineering Showcase competition
3. *Top Ten* – Texas Instruments National Design Competition
4. *Invited Presentation* – Bryan Software Developers Cartel
5. *Space Qualification* - RM-48 MISL Layer space qualified by NASA-JSC

Figure 9. MISL-ASEP Robot.

Based on these successes, a Fall2014/Spring 2015 Capstone team is now in the process of developing a cellular communications layer for the MISL stack. Although not currently of interest to NASA, there is a distinct possibility that this layer could be used for a number of earth-based system development projects in the other non-space-related environments. The Capstone team is also pursuing preparations for a KickStarter event to raise funding that would

support a startup company to commercialize many of the MISL layers and make them available to wide range of embedded systems developers. Their application will be a remote monitoring and control system using their cellular modem layer integrated into a MISL stack.

The MISL partnership has been a win-win proposition from its inception approximately one year ago. ESET students are now using space-qualified technology in their sophomore and junior level courses/laboratories with the plan to expand the MISL stack to other courses in the curriculum. In addition, the use of the MISL stack at the Capstone level will reduce hardware prototyping time. The private sector has also become increasingly more interested in the architecture from two different perspectives. First, is the use of the technology to support their own development efforts, and secondly to support sponsored projects to develop additional layers that could highlight their newly developed devices/modules.

Future plans are to look for opportunities to apply the MISL architecture to applied research and development. One interesting area where the MISL stack would be well suited is in the development of a new CubeSAT for low-cost space/reduced gravity research. Currently, there is no commercial solution available from a US company. The space-qualified and highly configurable aspects of the MISL architecture make it highly appropriate for this type of product development effort. The ESET Program is presently working with a small startup company to pursue this opportunity.

As the ASE Layer is integrated into the ESET curriculum and is used for the three-course sequence in embedded software development and possibly other courses such as instrumentation, control systems, networking, and communications, more Capstone projects will be able to take advantage of the architecture. This knowledge of and experience with the MISL layers and architecture with the associated data and power bus standards will add both to the development of new MISL layers as well as the application of the technology to a wider range of problem solutions.

Summary

Rarely are engineering technology programs offered the opportunity to participate in a long-term partnership with a government agency to design and develop a new architecture such as the Modular Integrated Stackable Layers. Lessons learned from the MISL development activities include:

1. Experience is highly motivational and rewarding for both the students and faculty involved.
2. Short-term value is primarily in new product development and applications
3. Long-term value is in continued support and migration of technology to other institutions and industry segments

The ESET Program continues to search for and identify funding to support the procurement of MISL layers in quantity. To date, the program has purchased three MISL layers in quantities of 100. These are

1. MSP 430 Layer
2. 802.11 Wireless Communications Layer
3. Analog System Evaluation Layer

Future purchases will include Power Layers and other wired/wireless communications layers. These layers will be used to support the three embedded software courses, the Capstone Design sequence, ongoing and future applied research projects, and to sell to other system developers. One interested customer is, of course, NASA. The organization will see a considerable cost and development time savings in being able to purchase MISL layers directly from the ESET Program rather than having to continue to acquire this technology using one-off procurement processes. If the current Capstone Design team is successful in using KickStarter to stand up a new company, the ESET Program will support this new venture with technical documentation and procurement support.

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