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Neuromorphic VLSI design course

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Hello

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This paper describes a novel Neuromorphic VLSI design course that was added to the Electrical and Computer Engineering curriculum at our university.

1. Significance

Neuromorphic VLSI design has been a research area for over 3 decades. It started with attempts at building silicon chips that could emulate functions of various brain regions like eye and cochlea [1]. With Moore's law hitting physical limits, the industry is looking to improve silicon circuit efficiency by exploring better algorithms like neurally inspired (neuromorphic). This includes Intel's foray into building neuromorphic chip, the *Loihi* [2]. This follows IBM's neuromorphic chip, the *True North* [3]. The *True North* is a neural processor with arrays of neurons and synapses. In addition to being a neural processor, the *Loihi* chip facilitates learning dynamically like the human brain. These chips can not only be used to emulate areas of the brain but also to build dedicated machine learning hardware [4] and to build neural prosthesis. Despite so many avenues, very few universities offer such a course. Therefore, we decided to offer this course at our university. This course includes teaching low power design, subthreshold mode circuits, mixed-signal chips, combining multiple chips into a system to realize neuromorphic hardware, background neuroscience and computational models.

2. Background

Neuromorphic circuits are inspired by the organizing principles of biological neural circuits. Computational elements of neuromorphic circuits are MOSFETs in sub-threshold mode operation. MOSFETs exhibit exponential I-V characteristics and low currents when operating in this mode. Adaptation, learning and memory are implemented locally within the individual computational elements like floating gates and MITES. Neuromorphic architectures often rely on collective computation in parallel networks. These properties lead to the feasibility of high-density, low-power implementations of functions that are computationally intensive in other paradigms. Application domains of neuromorphic circuits include neural prosthesis, building computational neuroscience models in silicon, machine learning processor, and applications of neural hardware like eye-camera.

Similar courses offered at Georgia Tech [5] and at the Institute of Neuroinformatics (INI), ETH Zurich [6] were studied to choose the topics appropriate for the course. Based on the study, topics to be covered in the course included: MOS transistors in CMOS technology, floating gates, static circuits, dynamic circuits, systems (silicon neuron-synapse arrays, silicon retina, silicon cochlea, silicon hippocampus, silicon lateral superior olive) with an introduction to multi-chip systems that communicate events analogous to spikes. This course was a 3-credit course, targeted at seniors and graduate students interested in machine learning, mixed-signal low-power VLSI design, neuroscience and neural engineering.

3. The course

a. Learning objectives/outcomes

Course objective was to understand the neuromorphic circuit elements as an emerging paradigm in VLSI circuit design. The learning objectives: basics of CMOS transistor operation- both above and subthreshold mode, basics of

neuroscience, computational model of neuron, synapse, various parts of the nervous system and to connect silicon neurons and synapses into systems representing parts of the nervous system like the retina, cochlea, hippocampus, etc. The learning objectives were reinforced with bi-weekly homework exercises that included small signal analysis of various circuits. Learning was tested in the midterm and final exams that were like homework exercises but closed book, closed notes. In the end of course project, students built neurally inspired silicon retina and demonstrated image processing by the retina.

b. Curriculum

This course covered devices in CMOS technology (MOS transistor below and above threshold, floating-gate MOS transistor, photo-transducers), static circuits (differential pair, current mirror, transconductance amplifiers, etc.), dynamic circuits (adaptive circuits), systems (silicon synapse, silicon neuron, silicon retina and cochlea, silicon lateral superior olive and hippocampal formation) and an introduction to multi-chip systems that communicate events analogous to spikes. Since it was an inter-disciplinary course, it taught students the basics of both VLSI circuit design and neuroscience like structure of neuron, synapse, retina, cochlea, hippocampus, and lateral superior olive. This was supplemented by study of the computational neuroscience models of these. The computational models were mathematical models, so they were translated to build silicon circuits in subthreshold domain.

Class Schedule

S.No.	**Topic**
1	Introduction to neuromorphic VLSI Systems
2	MOSFET Transistor Theory
3	Introduction to SPICE
4	Subthreshold Transistor Theory
5	Small Signal Analysis
6	Single transistor amplifiers
7	Current Mirrors (sub threshold)
8	Differential amplifiers (sub threshold)
9	Trans-amplifiers (sub threshold)
10	Elementary mathematical operations (subthreshold mode)
11	Log domain Integrators and differentiators (subthreshold mode)
12	Trans-linear circuit (subthreshold mode)
13	Diffusor circuit (subthreshold mode)

14	Winner-take-all circuit (subthreshold mode)
15	Bump and correlator circuit (subthreshold mode)
16	Synapse circuits
17	Neuron circuits
18	Address event representation circuit
19	Floating gates
20	MITES
21	Memristors
22	Lateral superior olive chip
23	Hippocampal Formation chip
24	Hippocampal Formation chip
25	Introduction to project
26	Biological retina
27	Photosensors
28	Silicon Retina
29	Silicon cochlea
30	See-hear chip
31-36	Project related inputs – report, circuits, PSPICE

c. Reference materials

Following three textbooks were referred to develop course materials.

*Analog VLSI: Circuits and Principles (*Shih-Chii Liu, et. al., 2002)

Analog VLSI and Neural systems (Carver Mead, 1989)

Analysis and Design of Analog Integrated Circuits, (Gray, Hurst, Lewis, Meyer, 5th Edition 2009)

These were supplemented with readings from literature on neuromorphic VLSI design, neuroscience and computational neuroscience.

d. Credits, hours, grading

This course was offered as a 3-credit hour, elective lecture course for students in Electrical and Computer Engineering, Bioengineering and Neuroscience. Pre-requisites included a course in circuit design and/or introductory course in neuroscience or permission of instructor.

Class meetings included 3 lectures weekly. Each lecture was an hour long. One hour of weekly lecture time for the initial 10 weeks was set aside for discussing homework problems in class. Group problem solving was encouraged in these

sessions. In the latter 5 weeks, project-based inputs were provided such as help with circuit design, PSPICE simulator and report writing.

Grading was based on homework assignments: 10%, exams (mid-term and final, both in class): 30% each, and end of term project: 30%. HWs were graded based on completion (not correctness). HWs were discussed in class as a teamwork exercise among groups of students. Total of 5 HWs, one every other week in the initial 10 weeks of the course were assigned. For the rest 4-5 weeks of the course, students worked on the project. Exams were closed book, closed notes, online (due to covid restrictions) with proctoring by instructors.

e. Lecture delivery

3 lectures of an hour each were delivered every week online via zoom. Some students attended the course from overseas. So, at times they could not attend the synchronous lecture. For their convenience, the lectures were recorded in zoom and the recordings were made available after the lecture. To avoid zoom bombing, students had to log in to their university zoom accounts to access the zoom session. Access to recordings was limited to students taking the course. A special course page was created for the same. Two samples of lecture slides are shown below.

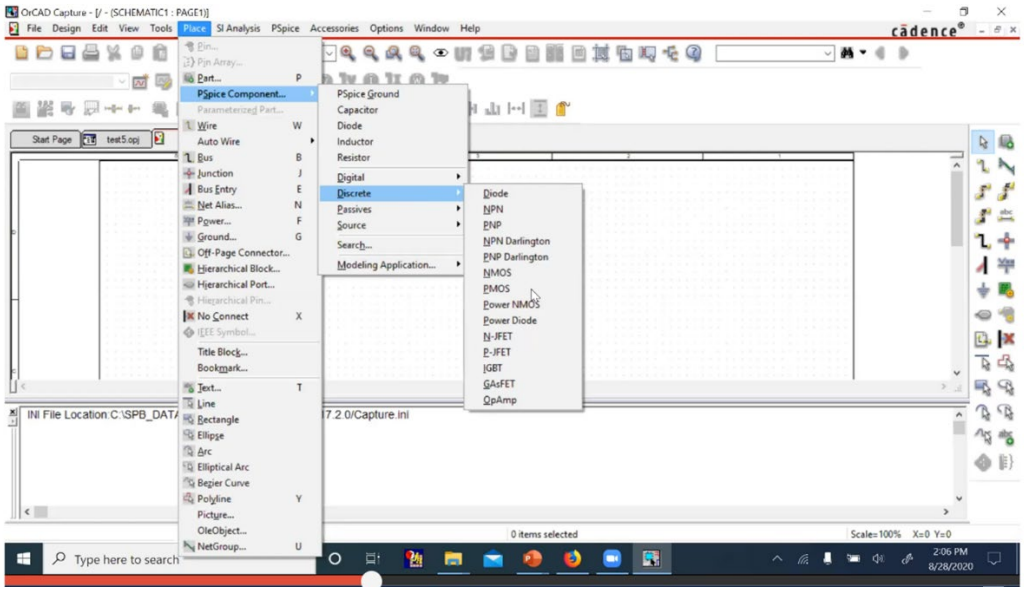


Fig. 1 Slide from lecture showing demonstration for PSPICE

One (Fig.1) is from the third lecture, when PSPICE use was demonstrated. The one in Fig. 2 is from one of the later lectures. It shows an online problem-solving exercise using power point slides. Students were assigned problems to solve at the beginning of the lecture as a group. They discussed the solutions in their groups and then presented them to everyone. The solutions were written on the slides or the white board in zoom.

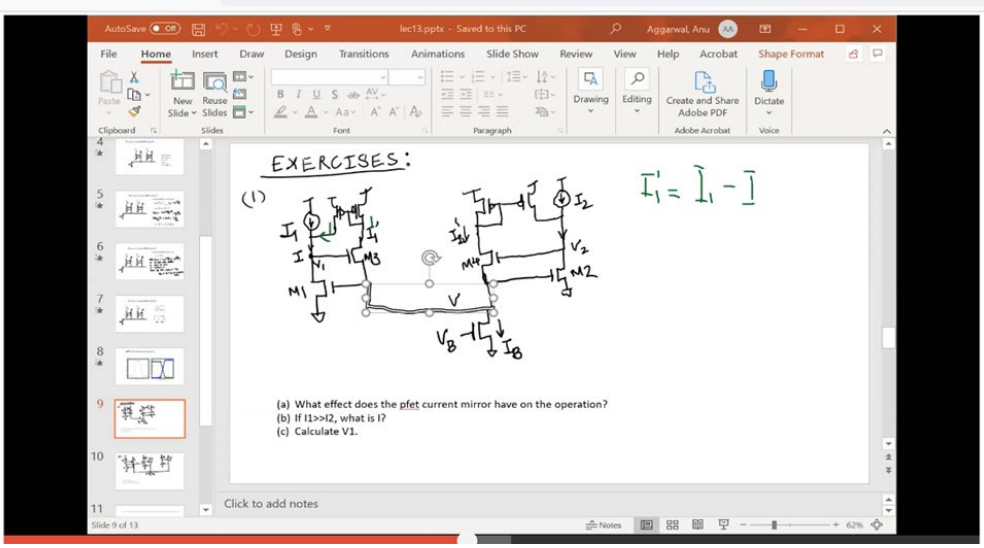
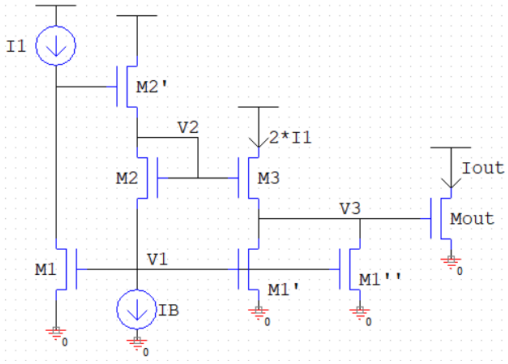


Fig. 2 Slide from a lecture showing problem solving exercise

f. Sample Homework/exam question

Five homework exercises were assigned through the course. One homework was assigned every two weeks. The homework included circuit design and analysis problems from the topics taught in the week. One of the problems and its solution is shown here for illustration. Students were required to solve the problem using circuit analysis principles taught in class including small signal analysis, sub threshold mode circuit analysis or PSPICE. The solutions were submitted online on blackboard.

Sample problem: Find Iout (in terms of I_B) in the following circuit operating in sub-threshold mode of operation.



Solution:

$$I_1 = I_o e^{\frac{kV_1}{U_T}}$$

$$I_B = I_o e^{\frac{kV_2 - V_1}{U_T}}$$

$$2I_1 = I_o e^{\frac{kV_2 - V_3}{U_T}}$$

$$I_{out} = I_o e^{\frac{kV_3}{U_T}}$$

If we apply the trans-linear principle and assume k=1,

$$I_1 I_B = 2 I_1 I_{out}$$

$$I_{out} = \frac{I_B}{2}$$

g. Project

Last four weeks of the course were dedicated to application of knowledge gained in the course to a project. The goal of this end of the term project was to design a silicon retina using sub-threshold mode VLSI circuits taught through the course. Students had to demonstrate use of this retina as a camera to process images. It was 4X4 pixel retina circuits (each pixel containing different layers - photoreceptors, horizontal cells, bipolar cells and ganglion cells) designed in PSPICE. With this silicon retina, a 4X4 pixel image with a 2X2 pixel object in it was processed by processing spatial intensity of all the pixels. This spatial intensity was processed to decode the object in the image. Based on this, the students had to derive an algorithm to detect the object from ganglion cell spikes.

Sample implementation of this project is presented here. It will demonstrate the key ideas and methodology for neuromorphic VLSI design taught in this course. And how these were applied by the students in this design.

Biology of retina

The retina of human eye works like a camera and has several layers of light processing cells – photoreceptors, horizontal cells, bipolar cells, amacrine cells and ganglion cells. To implement each pixel in silicon, one cell type from each of the layers needs to be implemented. Further, to port functionality of each cell in silicon, we need to understand its computational information processing. For instance, the photoreceptor converts light to electric current. So, photodiodes can be used to implement it in silicon retina. They also represent log conversion of intensity to current which is achieved by a transistor biased in subthreshold mode (where relationship between current and voltage is exponential). The next layer contains horizontal cells that allow current from several photoreceptors to be shared and smoothed. This can be designed using single transistors, the outputs of which are connected through a wire. The bipolar cell's output is proportional to the difference between the photoreceptor signal and the horizontal cell signal. Thus, bipolar cells can be designed in silicon using bump and anti-bump circuits or opAmp circuit. The ganglion cells produce spiking outputs proportional to the input current from bipolar cells. Thus, to model these in silicon, we can use the silicon circuit of an integrate and fire neuron.

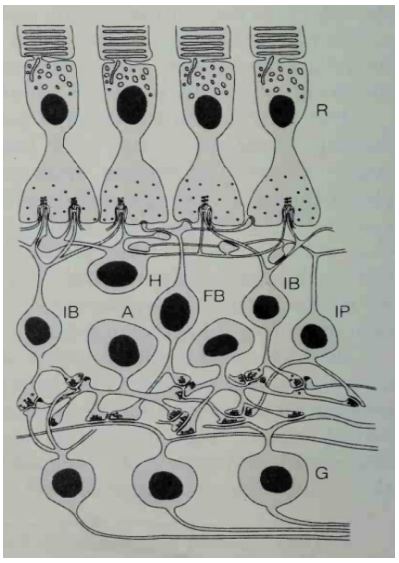


Fig. 3 biological retina – R-photoreceptors, H-horizontal cell, IB, FB, IP – Bipolar cell, A-amacrine cell, G- ganglion cell[1]

An example implementation of the silicon retina pixel from [1] is shown here.

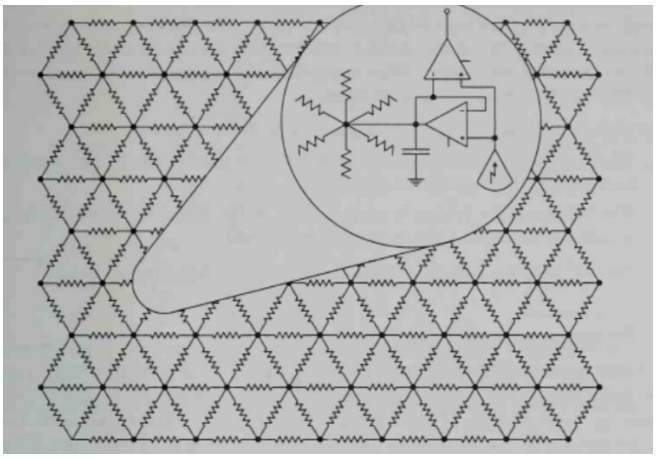


Fig. 4 Silicon retina example implementation (from textbook)

Sample project implementation

This section describes project of a group of students in the course. It describes the silicon implementation of different retinal cells and the algorithm to process their output.

Photoreceptor: was designed using three transistors on the left side (Fig. 5). The NMOS uses light inputs to stimulate the photodiode. The two diode-connected PMOS transistors transformed the output into the *"Vphoto"*.

Horizontal layer: The horizontal layer is shown in the middle part of the layout (Fig. 5). An opAmp was used as voltage follower to connect the *"Vphoto"* to the resistor network. Each pixel was connected through resistors to its six neighbors. The signal from a pixel's neighbors was connected as input "*Vavgin*". The pixel #6

is taken as an example. The six grey lines were connected to *"Vavg6"* net. This generated the average signal from neighbors of pixel #6 and goes into the "*Vavgin"* input of pixel #6.

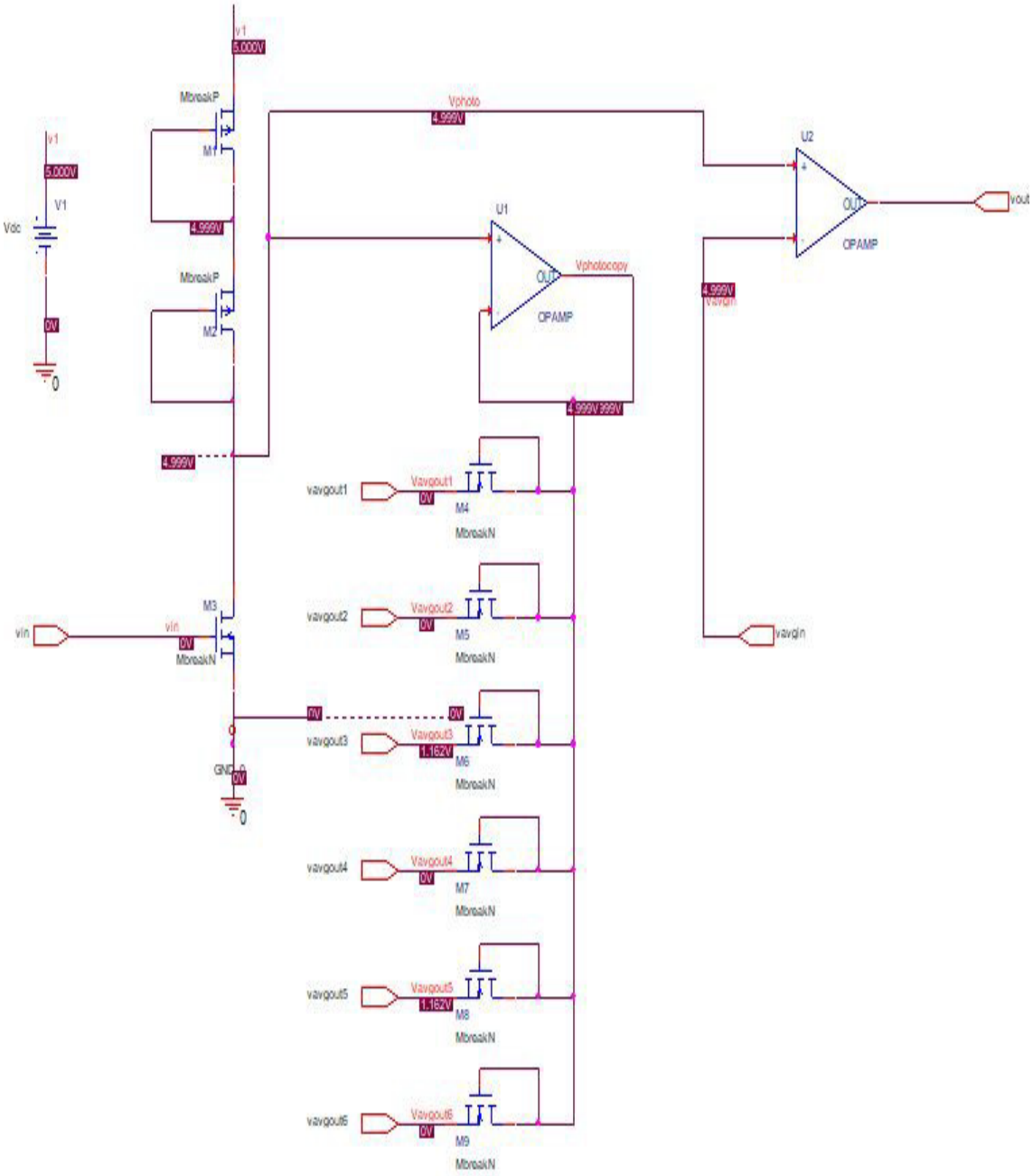


Fig. 5 circuit schematic of silicon retina pixel

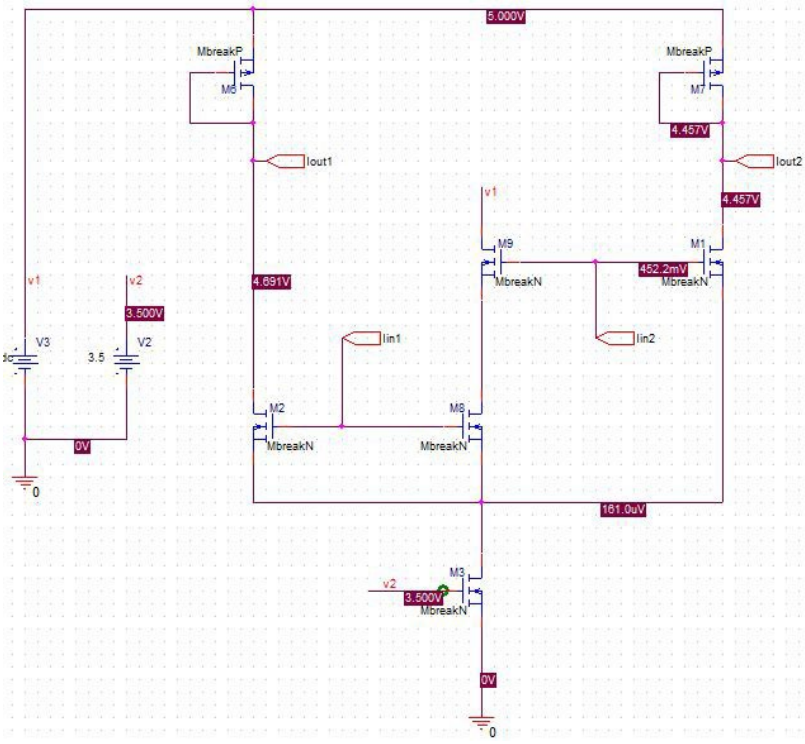


Fig. 6 Bipolar cell circuit schematic

Bipolar cell: The bipolar transistor compares the local average and the photo signal and provides an excitation signal to ganglion cells based on the comparison. A voltage mode bipolar cell using an opamp with an artificial gain of 1000 was used as bipolar cell (Fig. 6). The ideal opamp rejects all common mode signals and has linear gain across a wide range. When the photo voltage is smaller than the average voltage, the output is high at 4.2V, and when the photo voltage is higher than average voltage, the output is low at 3V.

Ganglion cell: an "integrate and fire" silicon neuron was designed to implement the ganglion cell (Fig. 7). The input voltage at 4.2V generated a constant charging current for the membrane capacitor, C2 and as it reached a potential comparable to the threshold of the invertors, the neuron fired spikes. Part of this voltage was fed back to maintain the membrane potential through capacitor C1 and part was used to discharge the potential to reset the neuron after a refractory period determined by Vrefr potential applied to gate of M8.

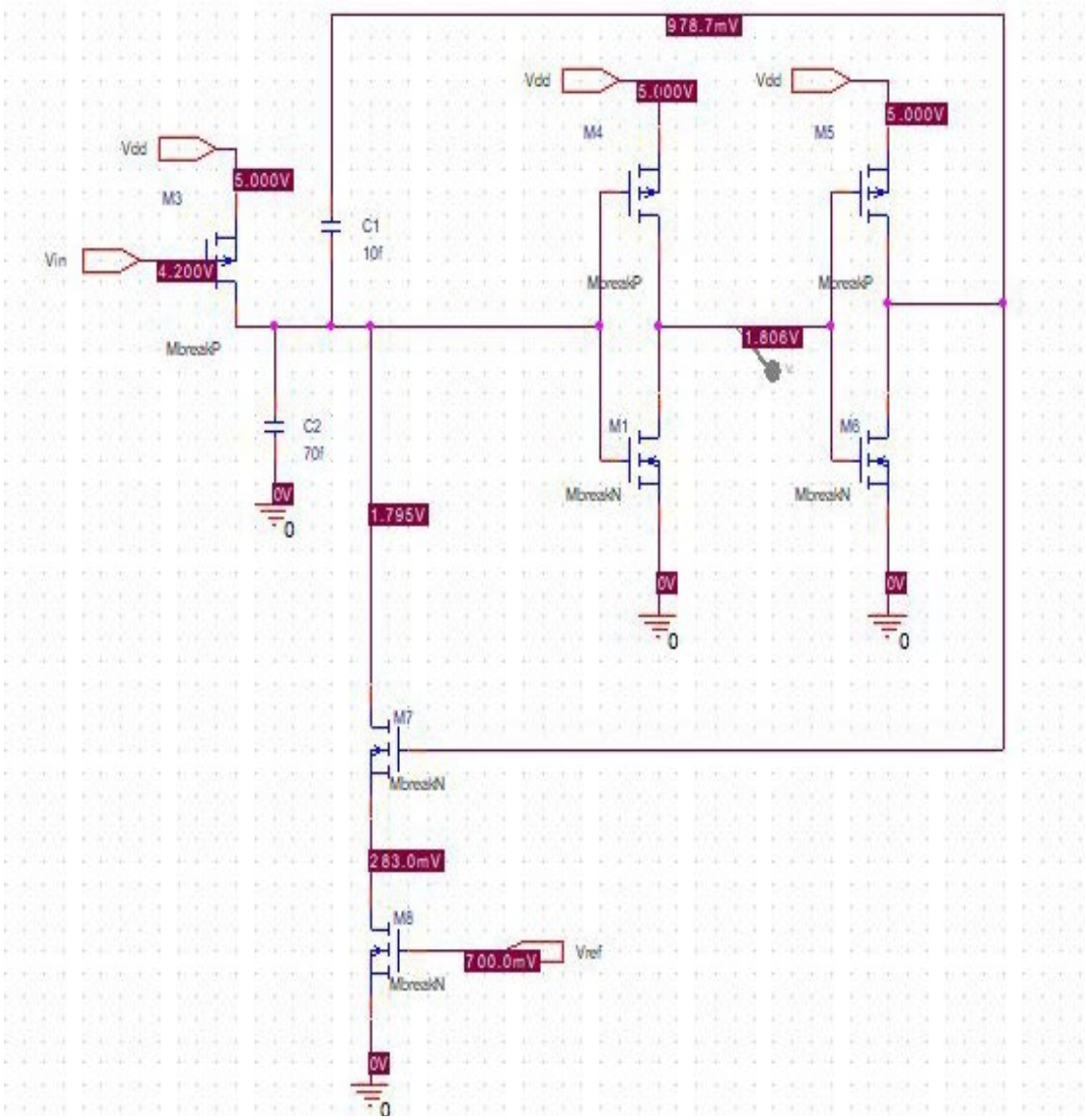


Fig. 7 Integrate and fire neuron as ganglion cell

System setup: A 4x4 pixel array was implemented and pixels were arranged hexagonally (Fig. 8). The input of 1 indicates light on the photodiode, and input 0 means no light input to the photodiode.

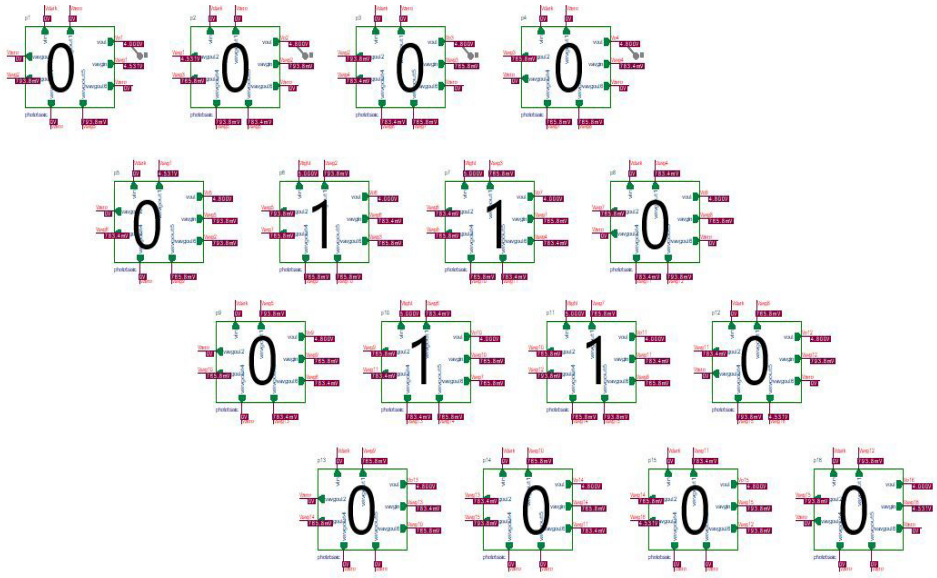


Fig. 8 4X4 pixel array

Photocurrent averaging and computing: The results are shown in the figure below. The *Vavgin* was the average intensity of neighbor pixels. When a neighbor did not exist, 0V was assigned as its input. For pixels with 0,1,2,3 illuminated neighbor pixels, the *Vavgin* varied between 0.73V to 4.53V. If the center cells had 1 as input, and its surrounding cells were partially illuminated, its response was higher than the average signal, and the output was 4.2V. This was the minimum voltage that can trigger a spiking output in the ganglion cell. For the pixels under dark condition, with one or more illuminated pixels around it, response is lower than the average signal, and the output is 3V, which is the neuron voltage at which C2 is being charged without neuronal firing. The ganglion cells output was periodic neural spiking from the activated pixels 6, 7, 10 and 11, (Fig. 9) and none from the inactive pixels.

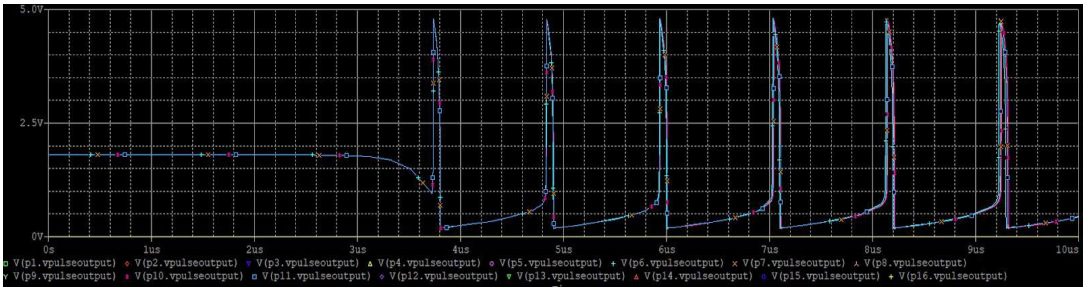


Fig. 9 Pulse signal from active pixels

4. Course outcomes

Course objectives to understand the neuromorphic circuit elements as an emerging paradigm in VLSI circuit design and learning objectives like learning the basics of CMOS transistor operation- both above and subthreshold mode, basics of neuroscience, computational model of neuron, synapse, various parts of the nervous system and to connect silicon neurons and synapses into systems representing parts of the nervous system were covered in the course

curriculum. Through various lectures, the students were taught topics like transistor operation in subthreshold mode. For each part of the nervous system implemented in VLSI design (including neurons and synapses), the topic started with its basic neuroscience structure and computational model which was later implemented in VLSI circuits. Their knowledge was tested through HWs, exams and the end of term project (samples shown above). Performance of students on various tests, especially the project, indicated that they had absorbed all the learning objectives. They used sub-threshold mode transistor circuits and knowledge of neuroscience to design parts of the nervous system. And used it for engineering applications like image processing. Upon completing the course, they have the skills to design any other part of the nervous system and use it for engineering applications.

All the students in this course performed well - 80% secured A grade and 20% secured B. None secured C or lower. In a comparable digital VLSI only course, with similar (seniors and graduate) student population and same instructor, 60% of the students secured A, 32% B grade and 8% secured C or lower grades. The difference could be because students who took this course had taken some VLSI course before (even though not a pre-requisite). Only the more committed students enrolled for the course as the content was more specialized and interdisciplinary (neuroscience and VLSI design). In student evaluation of the course, the rating of instructor and course content was much higher than that of comparable VLSI course.

5. Student population – interest group

Primarily, graduate students or final year undergraduate electrical and computer engineering students interested in VLSI design were enrolled in the course. This was a mixed signal VLSI design class; therefore, students had a broader learning experience. A new undergraduate neural engineering program has been started at the university. As the students reach their junior or senior year of the program, this course will be very useful for them. The students in neuroscience and neurology stand to benefit from it as well. The course starts with review of basic circuit concepts to bring neuroscience students up to speed. However, they will need a basic introductory circuit design course before taking this course. Students doing research in machine learning, interested in building their own data processor for faster and more efficient data processing could also be interested in this course.

6. Conclusion & Future work

The paper describes a mixed signal VLSI design course that was developed and offered to seniors and graduate students. It covered implementation of silicon neurons and synapses to build systems. It is useful in several ways – firstly, neuroscientists can build different parts of brain in silicon and model the working of systems of neurons and synapses. Secondly, some of the implementations could be used as prosthesis in patients with neural loss. Thirdly, machine learning and data processing algorithms could be implemented on silicon spiking neurons to conserve power and improve efficiency. Thus, this course can be a useful addition to the Electrical and Computer Engineering or Bioengineering curricula.

This course can be offered to students with more diverse interests viz., VLSI design, neural prosthesis, neural modeling, and machine learning. In future, we plan to introduce industry standard hardware like Intel's *Loihi* processor to implement the project. This will enable testing ideas on neuromorphic hardware before implementing in dedicated silicon chips which can be more economic.

7. References

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