

## PSpice Applications in the Teaching of Wireless and High Frequency Electronics

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### Abstract

The many recent technological developments in communication circuit design have paved a foundation for the development of complex personal communications systems. Although there are a variety of textbooks dealing with high frequency communication circuits and systems, there are very few sources of information integrating fundamental electronic circuits and components with overarching communication systems. A critical issue is the availability of inexpensive or free software that demonstrates the major circuit design considerations necessary for laboratories and projects. This paper has been written to relate our positive experiences using PSpice in a class entitled “High Frequency Electronics” (EE 626), which is a graduate level course at Oakland University in Rochester, Michigan. Examples discussed include the development and use of y- and s-parameter extraction circuits, Wilkinson power dividers and adders, directional couplers, baluns, hybrid rings, HF filters, and stability and load calculators. Several examples of circuit analysis using “PUFF” software have been added to illustrate microstrip implementations of the circuits analyzed with PSpice. A separate set of examples covering conventional communication circuits is presented in a companion paper entitled “PSpice Applications in the Teaching of Communication Electronics.”

### I. Introduction

Over the last decade, courses related to radio or high-frequency electronics have proliferated. One of the major reasons for such growth has been the skyrocketing interest in high-speed personal communication systems, which incorporate many electronic technologies.<sup>1,2,3</sup> However, problems related to the availability of inexpensive software and hardware come to the foreground in the development of more advanced (primarily graduate) courses that deal with high frequency electronics. The PSpice macromodules presented in this paper represent one method we have found to make high quality software modules available to our students using (for the most part) the free student demonstration version of PSpice. The macromodules chosen for this article are listed in Table 1. The high frequency electronics course is structured so as to include the topics shown in Table 2. The software used throughout the course includes PSpice, Matlab, and PUFF.<sup>4</sup>

Table 1: PSpice Macromodules Developed For High Frequency Electronics
a. Y-parameter extraction circuits
b. S-parameter extraction circuits
c. Wilkinson power divider/adder
d. Directional coupler
e. Hybrid ring
f. Balun
g. HF filter
h. Stability and load calculator

Table 2: Topics Covered in the High Frequency Electronics Course
1. Analysis of frequency and pulse behavior of basic lumped components with their parasitic elements.
2. Processes of component parameter identification based on frequency and time domain response.
3. Frequency and time-domain properties of transmission lines with time-domain reflections based on de Bergeron diagrams.
4. Frequency and time-domain operation of diodes and transistors
5. HF amplifiers; y, s, and ABCD parameters
6. HF oscillators (sinusoidal and pulsed); classical design and s-parameter design
7. HF communications circuits, including filters and mixers; modulators; demodulators,
8. HF speed logic circuits.
9. HF measurements and basic instruments such as spectrum analyzers and network analyzers.
10. Time domain reflectometry.

PSpice is conventionally used to perform circuit level simulations. However, the program can also be used in non-circuit applications, as we will discuss and demonstrate in this paper. For example, s- and y- parameters can easily be extracted from a transistor or circuit through use of a PSpice extraction macromodule. This involves the use of PSpice as a calculator, rather than as a circuit simulator. Examples of this latter use of PSpice are discussed in the sections explaining the y- and s-parameter extraction circuits and the load and stability calculator.

## II. Description of the PSpice Macromodules

### a. Y-parameter Extraction Circuits

Y-parameters become important at frequencies in the tens of MHz.\* As such, it is frequently necessary to characterize the y-parameters of transistors in these frequency ranges. A simple method of doing so is shown in Figure 1. The transistor under test (a MRF501 bipolar transistor) is at the center of the figure. On the left, in yellow, is the circuitry that provides an output voltage directly equivalent to  $y_{11}$ . This is accomplished by driving the transistor with one volt (voltage source V2).† Using 1.0 volt at this location makes finding  $y_{11}$  straightforward, because  $y_{11}$  is simply the current flowing through V2 divided by 1.0. The current through V2 is supplied as the control current of a current-controlled voltage source (CCVS). The voltage out of the

\* The relationship between voltage and current for the various types of parameters is reiterated here:

$$\begin{array}{lll} V_1 = h_{11}I_1 + h_{12}V_2 & I_1 = y_{11}V_1 + y_{12}V_2 & V_1 = s_{11}V_1^+ + s_{12}V_2^+ \\ I_2 = h_{21}I_1 + h_{22}V_2 & I_2 = y_{21}V_1 + y_{22}V_2 & V_2 = s_{21}V_1^+ + s_{22}V_2^+ \end{array}$$

At higher frequencies, the equivalent circuit of a transistor becomes a tangle of resistors, capacitors and inductors. The output impedance decreases from values in the kSs to fractions of kS's. H-parameters, which are obtained by opening and shorting the outputs of the device under test, are easy to obtain for transistors up through frequencies of a few MHz. From several MHz to approximately 100 MHz, y-parameters are easier to obtain, since they involve only the use of shorts (open circuits are virtually impossible to obtain because of capacitive effects). Above 100 MHz, it is easiest to use s-parameters, because it is difficult to obtain either an open or a short at the output with those frequencies.

† Note that in real electronic circuits, 1.0 volt input would overdrive the transistor. However, PSpice works by taking only the small signal (differential) parameters of the transistor at the DC operating point. Therefore, the simulation complacently operates with the "improper" 1.0 volt input. It might also be asked why a current probe is not used instead of the CCVS. Current probes in PSpice have to be carefully placed in order to show the correct current direction. The circuit shown avoids the hassles of current probe placement.

CCVS is directly equal to  $y_{11}$ .  $Y_{21}$  is obtained in a similar manner through the portion of the circuit shown in orange on the left. Notice that no voltage source is required on this side, since only transmitted voltage and current values are being assessed. The values for  $y_{11}$  and  $y_{21}$  as a function of frequency are shown in Figure 2. Here it can be seen that the input admittance rises as a function of rising frequency, while the transadmittance falls.

Figure 3 shows a  $y_{22}$  and  $y_{12}$  parameter extraction circuit. The 1.0 volt source has simply been swapped to the other side of the transistor. The magnitudes and phases of the parameters as a function of frequency are shown in Figure 4.

### b. S-parameter extraction circuits

The two circuits shown in Figure 5 are assembled to determine the s-parameters for the MRF501 bipolar transistor. The operating point of the transistor is  $I_E=5\text{mA}$ , with  $V_{CE}$  close to 12V. The upper circuit extracts  $s_{11}$  and  $s_{21}$ , while the lower circuit extracts  $s_{22}$  and  $s_{12}$ . The s-parameters can be read from PSpice and transferred to other programs, such as PUFF. S-parameters extracted from the transistor are shown as a function of frequency in Figure 6.

The internal structure of modules HB1 and HB5 of Figure 5 are shown in Figure 7. Here a 1.0 volt sinusoidal source (V1) is applied through a 50  $\Omega$  resistor to the input of a voltage controlled voltage source (VCVS). This input is also connected, through the external connector labeled 'SRMS,' to a 50  $\Omega$  termination leading to the external connector labeled 'GROUND.' The input of the VCVS is therefore 0.5 V. Since the gain of the VCVS is 2, it follows that V2 must have an amplitude of 1.0 V. The voltage difference between V2 and ground is therefore precisely equal to either  $s_{11}$  or  $s_{22}$ , depending on where the block is placed in the circuit. For example, a short will indicate a voltage, and reflection coefficient, of  $-1$ , while an open will indicate a voltage, and reflection coefficient, of 1.0.

A similar circuit showing the internal structure of modules HB2 and HB3 of Figure 5 is shown in Figure 8. This circuit is used to test  $s_{21}$  and  $s_{12}$ . A 1 volt source is assumed to be supplied through a 50  $\Omega$  resistor to the external connector labeled 'XTRANS.' Thus the VCVS is supplied with 0.5 volts at its input. Since the gain of the VCVS is 2, the output sent to the external connector XTRANS should be 1.0, which would also be precisely equal to the  $s_{12}$  or  $s_{21}$  value expected for that set of inputs. Any deviation from the expected 1 volt with 50  $\Omega$  circuitry on circuit external to the XTRANS connector will produce an output voltage directly proportional to  $s_{21}$  or  $s_{12}$ .

Table 3: PSpice Parameters for the MRF501		
$I_s = 69.28 \text{ E-18}$	$B_r = 1.143$	$C_{je} = 939.88 \text{ fF}$
$X_{ti} = 3$	$N_c = 2$	$M_{je} = 0.0453$
$E_g = 1.111$	$I_{sc} = 0$	$V_{je} = 0.75$
$V_{af} = 100$	$I_{kf} = 0$	$T_r = 1.5744$
$B_f = 288.5$	$R_c = 4$	$T_f = 141.2 \text{ p}$
$N_e = 1.186$	$C_{jc} = 893.1 \text{ fF}$	$I_{tf} = 0.27$
$I_{se} = 69.28\text{E-18}$	$M_{jc} = .3017$	$V_{tf} = 10$
$I_{kf} = 22.4 \text{ m}$	$V_{jc} = 0.75$	$X_{tf} = 30$
$X_{tb} = 1.5$	$F_c = 5$	$R_b = 10$

The parameters of the transistors are described in terms of the SPICE Gummel-Poon model, as illustrated in Table 3.<sup>5,6</sup> Four of these values:  $T_r$ ,  $T_f$ ,  $C_{je}$ , and  $C_{jc}$ , form the fundamental parasitic values affecting the calculations PSPICE performs in evaluating the s-parameters of the transistors. Consequently, the extraction circuits can be used to check how parasitic components affect the s-parameters. Another application that has been explored involves the modification of SPICE

parameters of a transistor to achieve assumed s-parameters by changing transistor capacitances and transition times. The four important parasitic parameters noted above can also be changed within PSPICE to reflect values of transistors that happen to be handy in the laboratory, so that s-parameters can be found for the actual components students plan to use in laboratory circuits. Table 4 shows parasitic parameters for a number of common transistors.

Connecting a transistor to a network analyzer can produce noticeable deviation in s-parameter values due to the effects of the cables.<sup>7,8,9</sup> This effect can be demonstrated as shown in Figure 9, where transmission lines have been attached to the input and output connectors. Although these transmission lines are lossless, they provide a good feel for the phase shifts that occur due to their presence. Figure 10 should be compared with Figure 6 to see this difference.

Table 4: Comparison of parasitic parameters in common transistors					
	2N5109	PN5179	2N5179	2N3478	MRF501
$T_r$	20 n	1.588 n	1.588 n	1.615 n	1.574 n
$T_f$	0.1 n	141.1 p	135.6 p	140.9 p	141.2 p
$C_{je}$	10 p	939.8 f	1.52 p	939.8 f	939.8 f
$C_{jc}$	5 p	893.1 f	1.42 p	893.1 f	893.1 f

### c. Wilkinson Power Divider

The Wilkinson power divider delivers source power from one source to two or more loads, minimizing reflections and providing for good separation of the outputs (Figure 11). Figure 12 shows the voltages of the power split as a function of frequency. The signal from a 50-ohm source is split between two quarter-wave transformers (transmission lines) to minimize reflections. The outputs are two 50  $\Omega$  loads. The 2.5 ns delay on the 70  $\Omega$  lines corresponds to  $\pi/4$ . The same line connections can be used to add powers, as will be shown later.

The reflection and transmission parameters can be tested using s-parameter blocks, as shown in Figure 13. The power is designed to flow from the leftmost port to be split evenly between the two rightmost ports, as indicated by the purple arrows. Reflections back into the input port, (the red arrow on the figure), are to be minimized at the frequency for which the circuit was designed. This is proven out by the plots of Figure 14. The s-parameters for the ports are precisely equal to the indicated voltages.  $V(s11)$  is a minimum at the design frequency of 100 MHz, while  $V(s21upper)$  and  $V(s21 lower)$  are at a maximum.

Additional s-parameter tests of the Wilkinson circuit are shown in Figures 15 and 16. This time the circuit is tested as a potential signal adder. The HB1 and HB3 s-parameter testing blocks were swapped from the configuration of Figure 13 so as to test for isolation between the two ports on the right (Figure 15). (The HB1 block contains the voltage source used for testing, so a voltage source is being input to the bottom right port in this new configuration.) Simultaneously, this new configuration tests the isolation between the lower right hand port and the connection back to the port on the left. The red arrows on the figure indicate minimal power flow in direction indicated, while the purple arrow indicates that power can flow freely in the indicated direction. The s-parameters are shown as a function of frequency in Figure 16. In this case,  $V(S21left)$  is the right-to-left transfer parameter,  $V(S11)$  is the lower right port reflection parameter, and  $V(S21upper)$  is the transfer parameter indicating output-to-output transfer.

The PSPICE simulations of this macromodule are primarily used to demonstrate circuit principles and to observe the effects of changes in major circuit parameters. Another inexpensive

program, PUFF, can be used as an extension of the PSpice simulations in order to include microstrip technology with substrate and strip conductor parameters. Figure 17 illustrates the same Wilkinson power divider as analyzed using PUFF. Notice that the PUFF circuitry is scaled to 1 GHz, corresponding to thin film technology.

The Wilkinson power divider applied as a power adder is shown in Figure 18. In this case two previous 'outputs' on the right become the new inputs for two sources. The new output moves to the left-hand side. The voltage outputs for this configuration are shown in Figure 19—clearly powers are adding as expected at the design frequency. Isolation for this circuit can be investigated through the use of s-parameters, as discussed above. In general, these simulations can be easily expanded in order to test circuit tolerances, bandwidth, and other important characteristics.

#### **d. Directional Coupler**

Figure 20 illustrates the schematic design for a directional coupler operating at 100MHz. This is a version of the so-called 'branch-line coupler' typically used in microstrip technology.<sup>10,11,12,13</sup> Sections of transmission line forming the square have  $\frac{1}{4}\lambda$  lengths. This length corresponds to 2.5 ns delay time for 100 MHz. Horizontal branches of the square are set at  $36\ \Omega$  to obtain the desired attenuation and to minimize reflections. The corresponding output plot of Figure 21 illustrates how power is transferred from one port (port 2) to the two other ports (3 and 4). There is some attenuation in this transfer (3dB in voltage or 6dB power), with about 17dB power attenuation or rejection in relation to power transfer to port 1. The reflection and transfer functions are detected by means of the circuit shown in Figure 22, and the s-parameter test results in Figure 23.  $S_{42}$  and  $S_{32}$  show the forward transfer functions, while  $S_{12}$  indicates the reverse transfer function—the coupler directivity indicator or rejection factor.  $S_{22}$  is the reflection coefficient observed at the input terminals. By simply exchanging the HB1 and HB3 blocks, as was done on the Wilkinson power divider, other important parameters can be found. The same type of a coupler is simulated with PUFF in Figure 24.

#### **e. Hybrid Ring (Rat-race Circuit)**

The hybrid ring (rat-race) circuit operates in such that if a signal is applied to port 1, it is split evenly into two in-phase signals with a  $180^\circ$  phase difference at ports 3 and 4, while port 2 is isolated (Figures 25 and 26). This structure, designed to operate at 100MHz, is a model of a microstrip implementation that usually operates at higher frequency (Figure 27).

#### **f. Balun**

A balun is a device that provides a transition between an unbalanced transmission line and a balanced, or symmetric, transmission line. As shown in Figure 28, a signal is sent from a source through a  $70\ \Omega$  unbalanced transmission line (grounded outer connector) to a  $300\ \Omega$  balanced (symmetric) transmission line connected to a  $300\ \Omega$  resistor (this represents a loop antenna). The inputs of the balanced line are separated by a  $70\ \Omega$  unbalanced section of half-wave length cable. This introduces a  $180^\circ$  phase shift between the signals at its end that serve to drive the balanced line (Figure 29). The same principle can be used to connect a balanced receiving antenna to an unbalanced transmission line that is connected to a receiver.

### **g. HF Band-Pass Filter**

An HF band-pass filter designed ‘by intuition’ is shown in Figure 30. Either the top or the bottom transmission line serves as a short (due to cable length and impedance) at the frequencies where the filter shows a minimum (Figure 31). Both stubs are open at the frequency of maximum transmission.

### **h. Stability and Load Calculator**

It is often important to find the potential instability conditions of transistors, as well as load and source impedances to achieve a desired gain. A sequence of calculators is being developed to simplify the tedious and involved computations, which are often based on complex variable expressions. The input variables to these calculators are primarily s-parameters, which can be determined using the s-parameter extraction circuits previously described, or obtained directly from data sheets. The calculator we present here—Calculator I—is intended to illustrate the idea of applying PSPICE as a sophisticated analog computer that can help solving various types of equations, including integral and differential equations.

Calculator I (Figure 32) computes the Stability Factor (SF), as well as the circle centers, radii, and distances of the centers from the origin of the Smith Chart of the Source (Cs) and the Load (Cl) stability circles. The circles can then be placed in the Smith Chart to determine stable operating conditions, which is important when the stability factor is less than 1. In this latter case, the load and source power circles can be plotted and stable load and source conditions selected to achieve the desired gain, (if it is achievable). If the stability factor is greater than 1, the transistor is unconditionally stable, and further calculations can be performed to maximize the gain or meet other goals. The complex interior structure of Calculator I is indicated in Figure 33.

Calculator I can be also used in close conjunction with the s-parameter extractor. This technique is especially helpful when transistor instability detected by the calculator ( $SF < 1$ ) is to be corrected by connecting “damping” resistors in series or in parallel with the transistor base terminal. In this case, a new s-parameter set is entered into the calculator, and stability conditions are tested again. For an unstable transistor, it is recommended that stability circle parameters, calculated by means of Calculator I, be transferred to the Smith Chart. Selection of the operating conditions would then take place. Other calculators, currently under development, are planned to automate several other steps of amplifier design, such as computations of load and source network parameters for desired amplifier gain.

## **III. Conclusions**

PSpice can be an extremely effective pedagogical tool for high frequency applications. It is useful in explaining and bringing to life conventional HF circuitry such as Wilkinson power dividers and adders, directional couplers, baluns, hybrid rings, and HF filters. The examples demonstrated here can be easily expanded to test circuit parameter sensitivities and tolerances. PUFF, an inexpensive program for microstrip-type simulations, is a useful supplement for the enhancement of PSpice macromodules. Perhaps surprisingly, PSpice is also very useful in applications complex calculations. Stability and load calculators, as well as y- and s- parameter extraction circuits, have been devised and successfully used in laboratories and projects. The

use of instructor-devised PSpice macromodules for high frequency electronics related courses can greatly extend students' understanding and design capabilities in a complex discipline at very low cost.

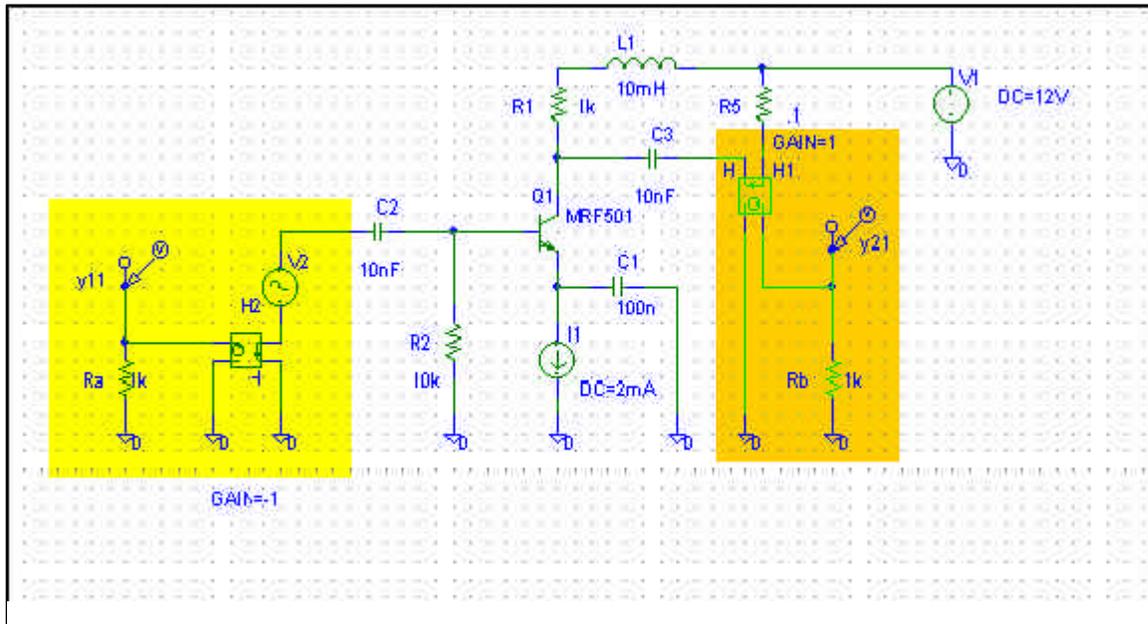


Figure 1:  $y_{11}$  and  $y_{21}$  parameter extraction circuit.

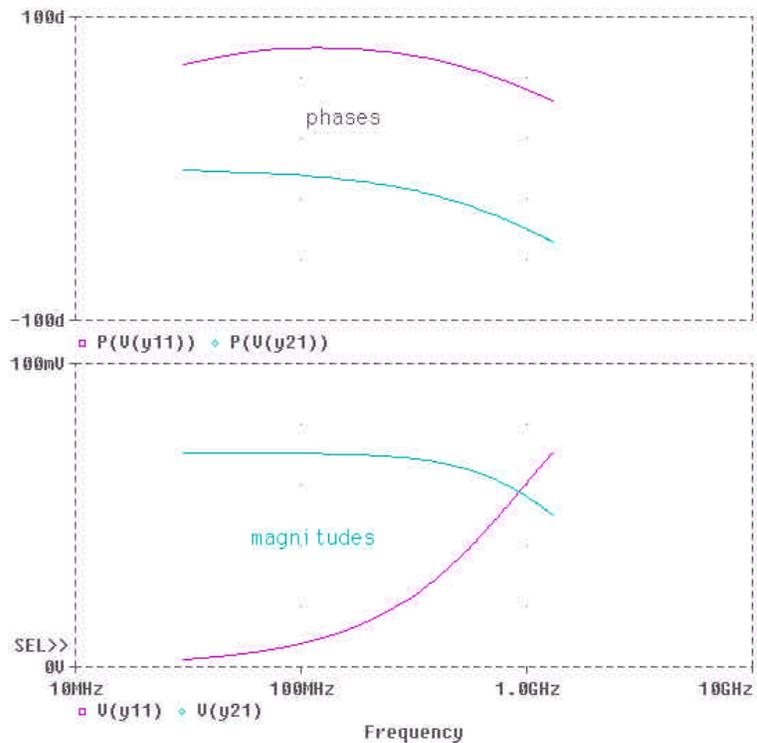


Figure 2:  $y_{11}$  and  $y_{21}$  as a function of frequency.

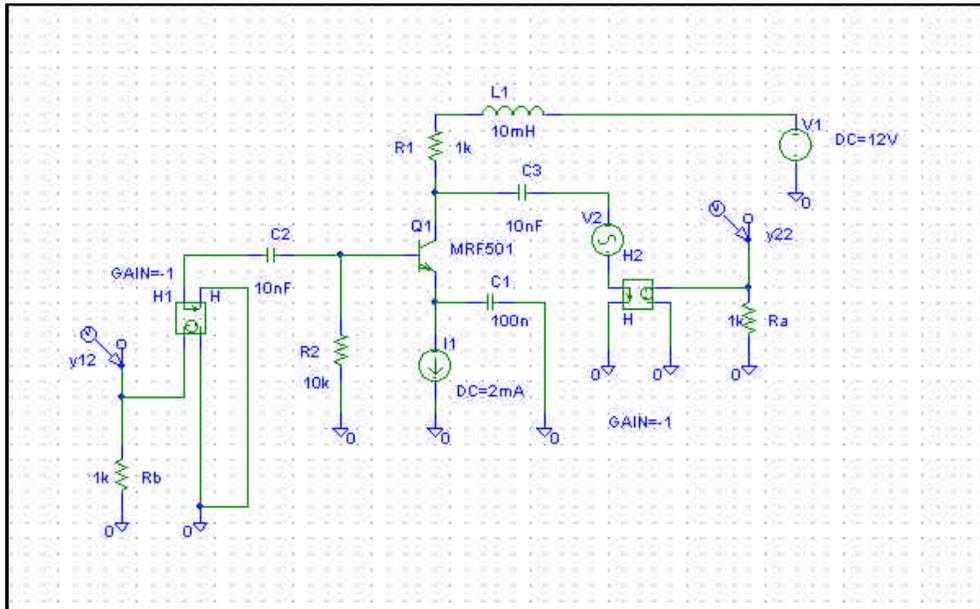


Figure 3:  $y_{22}$  and  $y_{12}$  parameter extraction circuit.

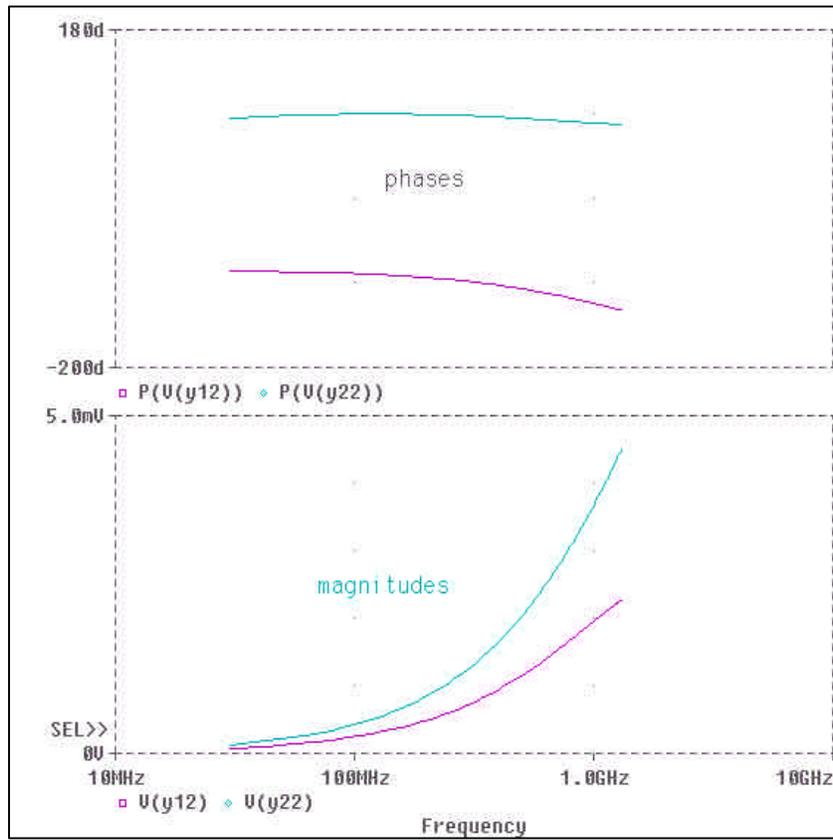


Figure 4:  $y_{22}$  and  $y_{12}$  as a function of frequency.

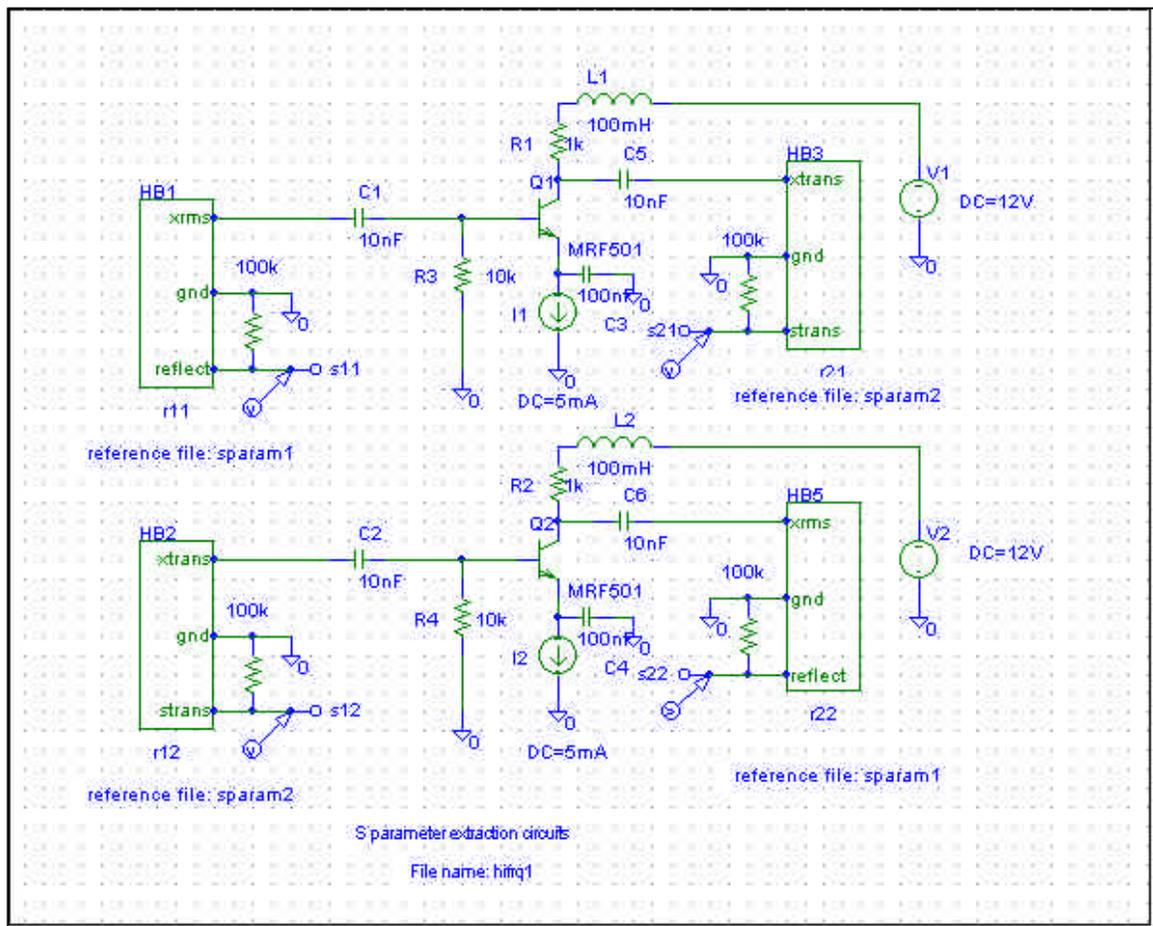


Figure 5: S-parameter extraction circuits.

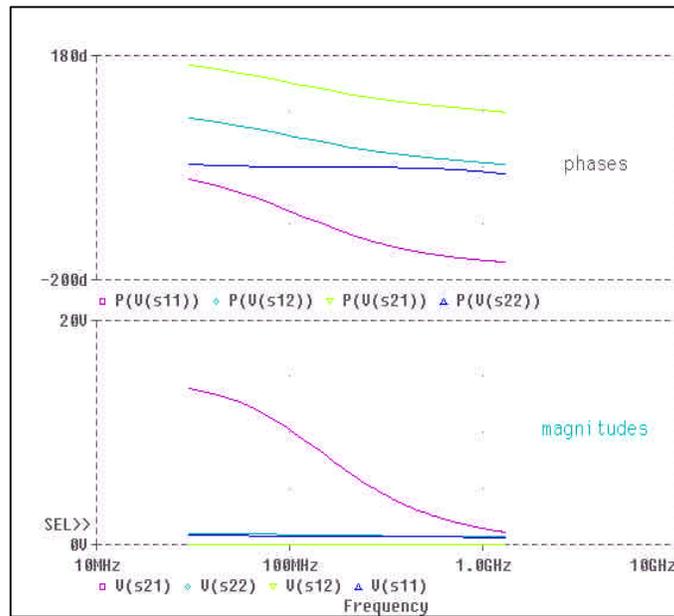
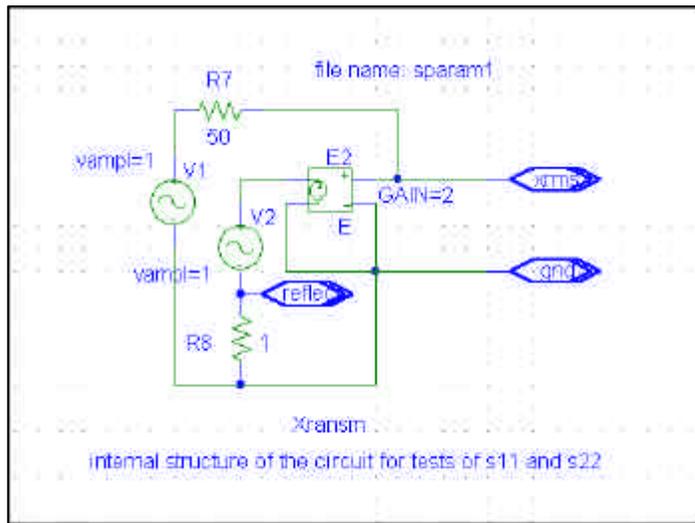
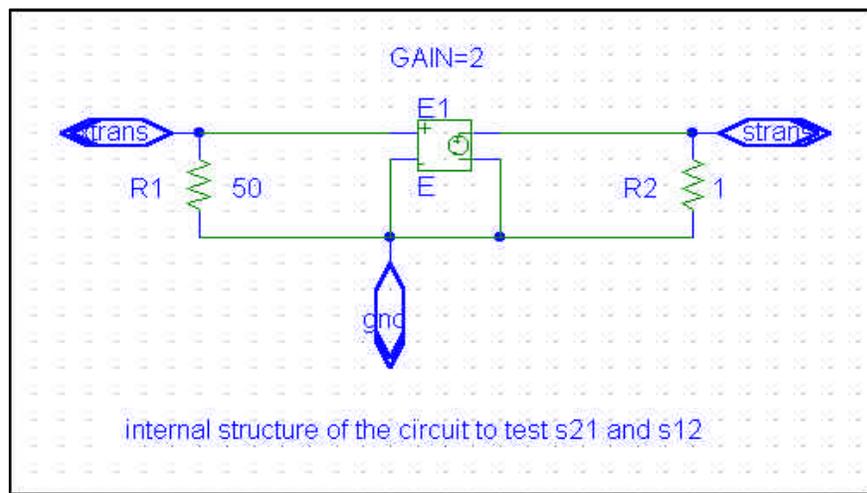


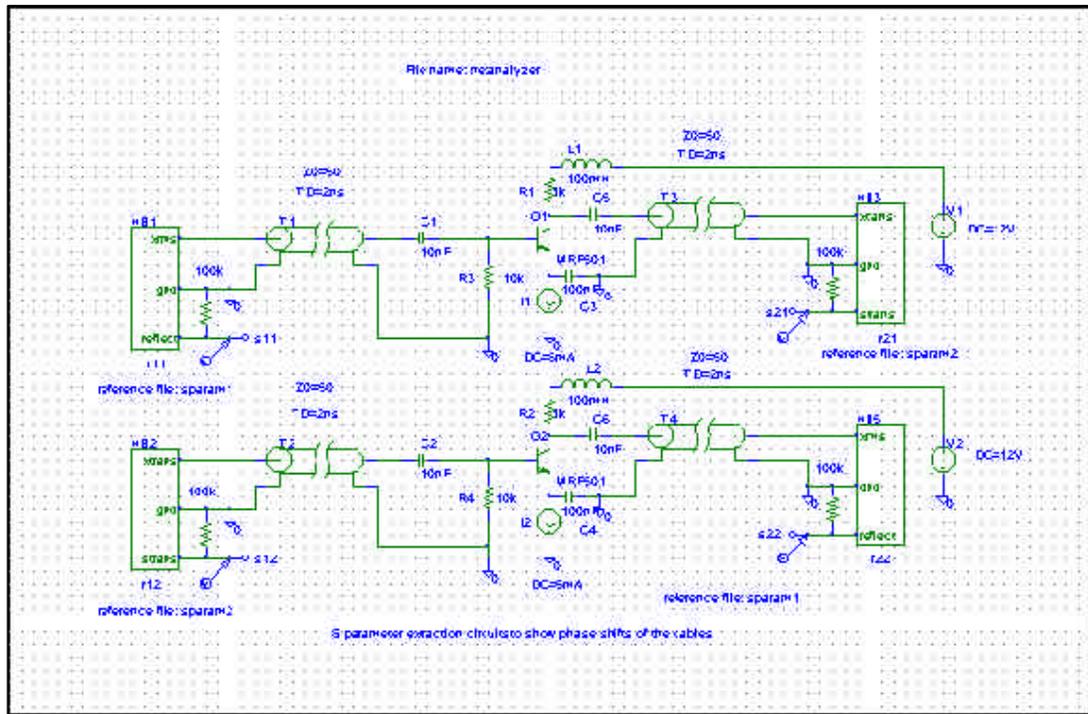
Figure 6: Magnitude and phase as a function of frequency of  $s_{21}$ ,  $s_{22}$ ,  $s_{12}$ , and  $s_{11}$ .



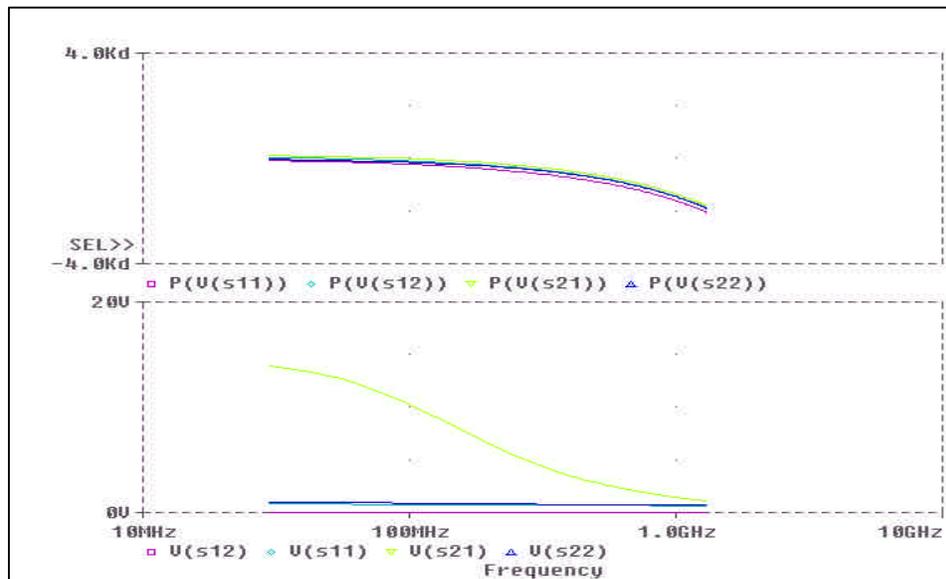
**Figure 7:** Internal structure of the circuit used for tests of  $s_{11}$  and  $s_{22}$ .



**Figure 8:** Internal structure of the circuit used to test  $s_{21}$  and  $s_{12}$ .



**Figure 9:** S-parameter extraction circuits with added transmission lines to simulate the effects of cables used in network analyzers.



**Figure 10:** Magnitude and phase of s-parameters in circuit with added transmission lines to simulate the effects of cables used in network analyzers. Compare this figure with Figure 6.

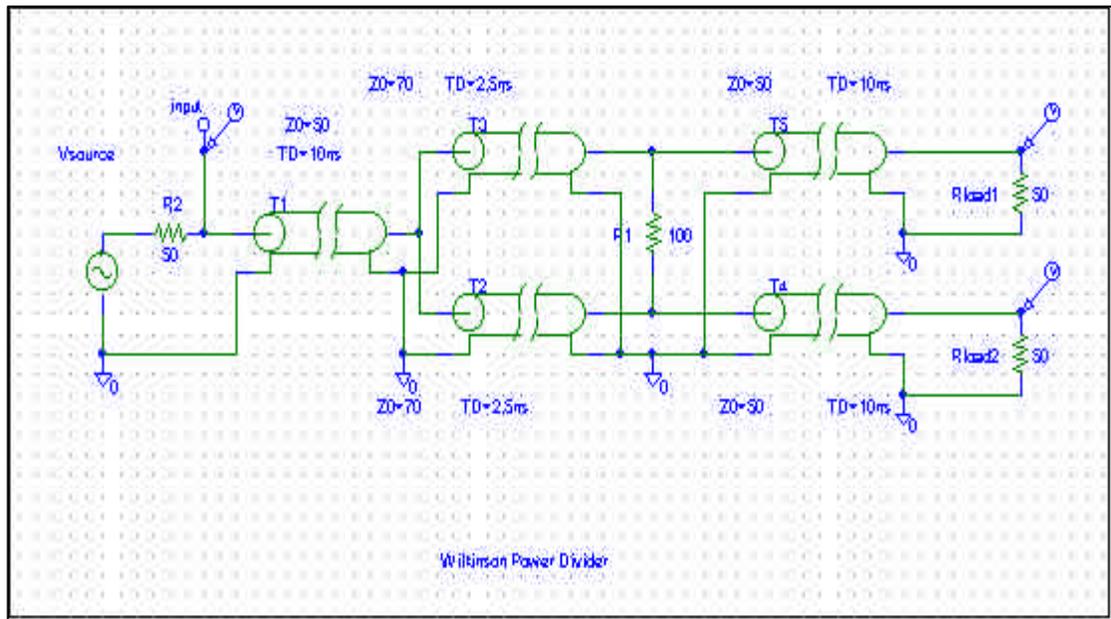


Figure 11: Wilkinson power divider.

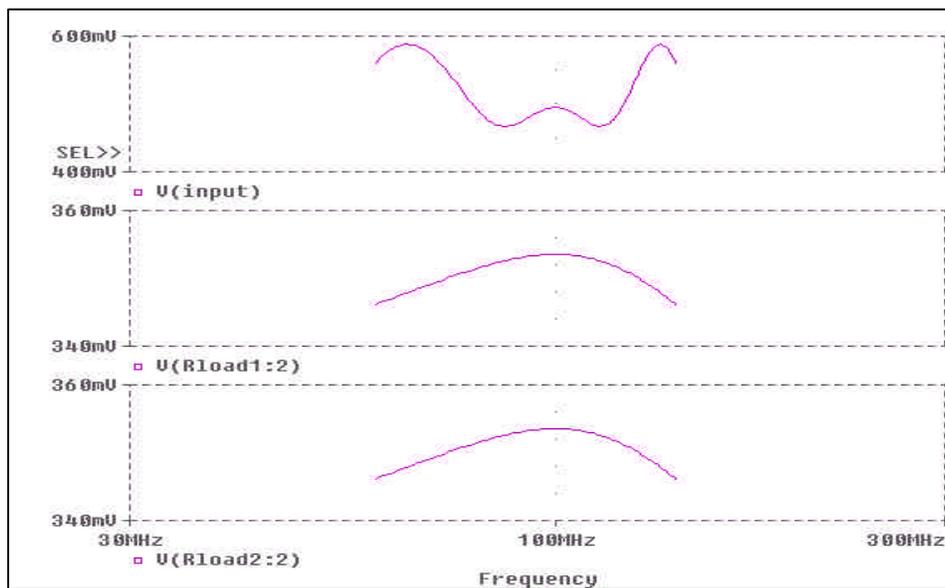
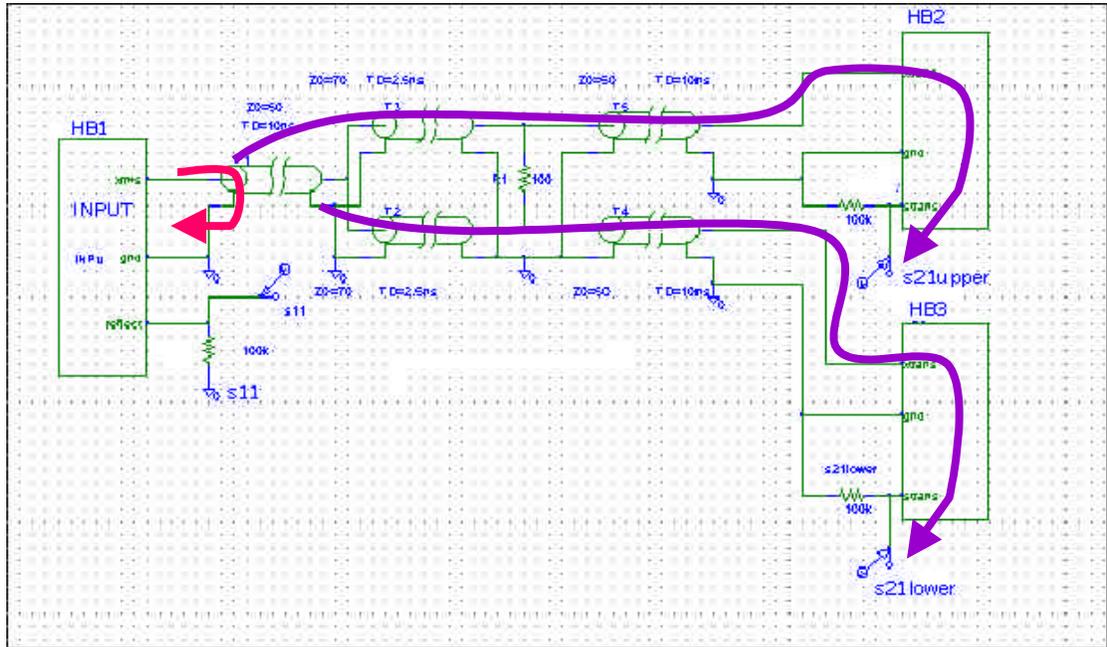
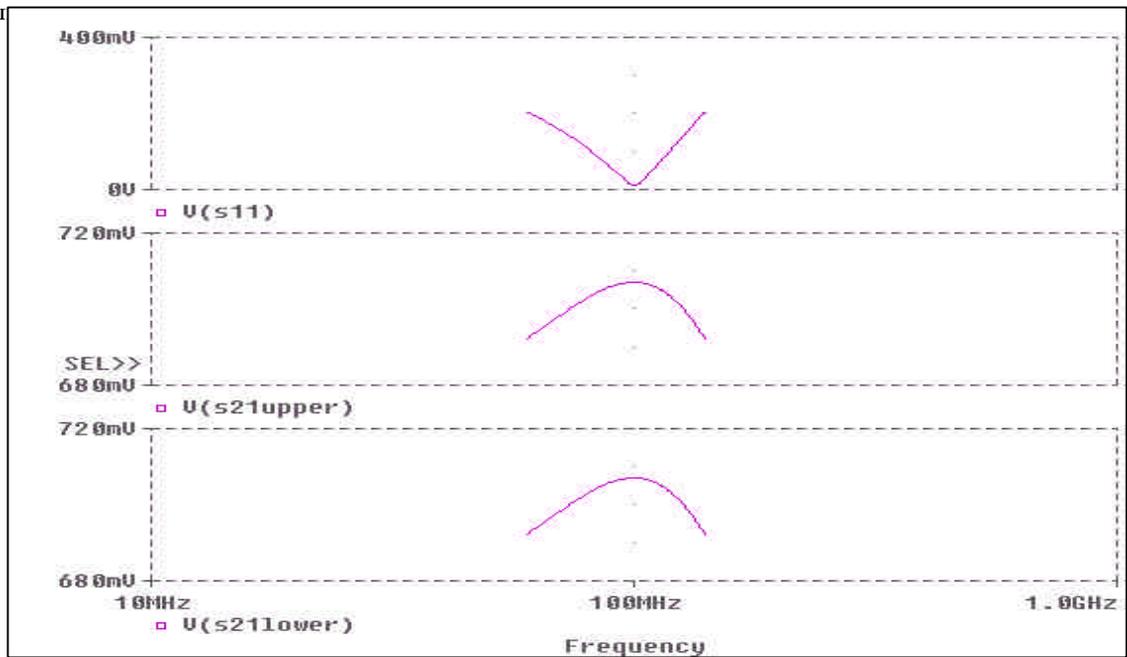


Figure 12: Voltages of the Wilkinson divider power split as a function of frequency.

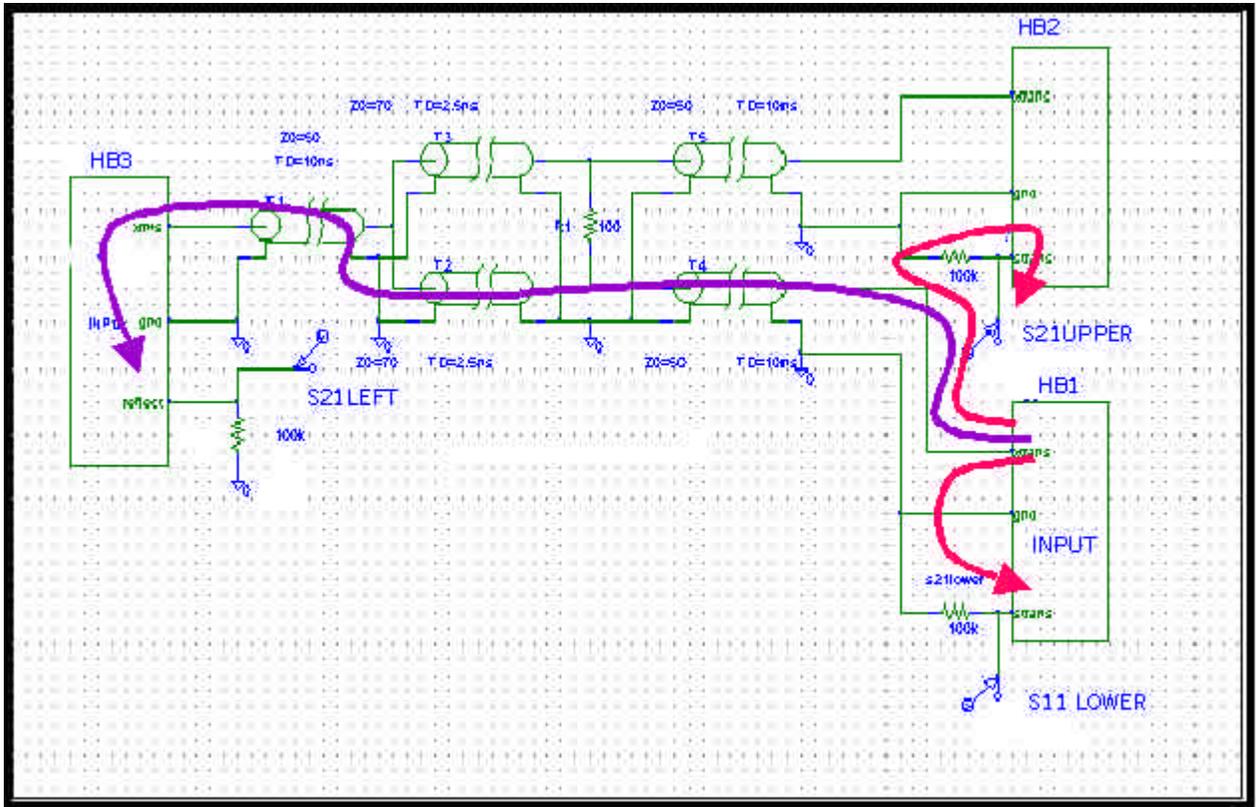


**Figure 13:** Wilkinson divider with s-parameter extraction blocks. Purple arrows indicate direction of power flow at that frequency, while the red arrow indicates minimal reflection of power directly back from the input terminal.

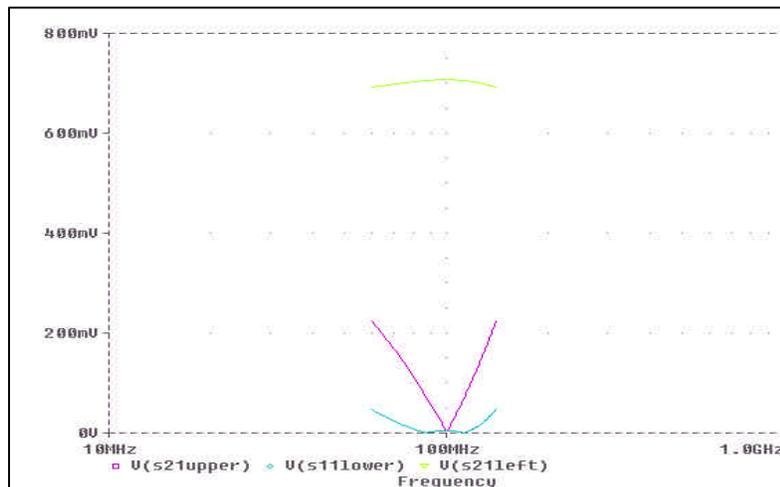
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**Figure 14:** Voltages of the Wilkinson divider, which are directly proportional to the respective s-parameters, as indicated.  $V(s_{11})$  is a minimum at the design frequency of 100 MHz, while  $V(s_{21upper})$  and  $V(s_{21lower})$  are at a maximum.



**Figure 15:** Additional s-parameter tests of the divider . The HB1 and HB3 s-parameter testing blocks were swapped from the configuration of Figure 13 so as to test for isolation between the two output ports on the right. (The HB1 block contains the voltage source used for testing, so a voltage source is being input to the bottom right port in this new configuration.) Red arrows indicate minimal power flow in that direction, while the purple arrow indicates that power can flow freely in that direction.



**Figure 16:** Voltages of the Wilkinson divider with test setup as shown in Figure 15. The s-parameters are directly equal to the respective voltages.

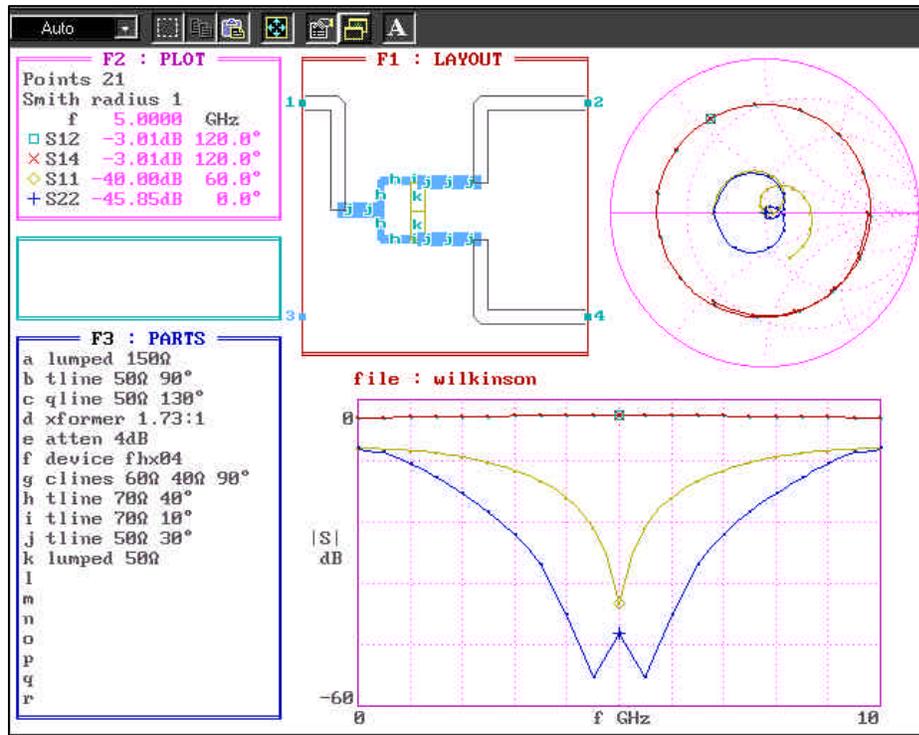


Figure 17: Wilkinson power divider as analyzed by PUFF.

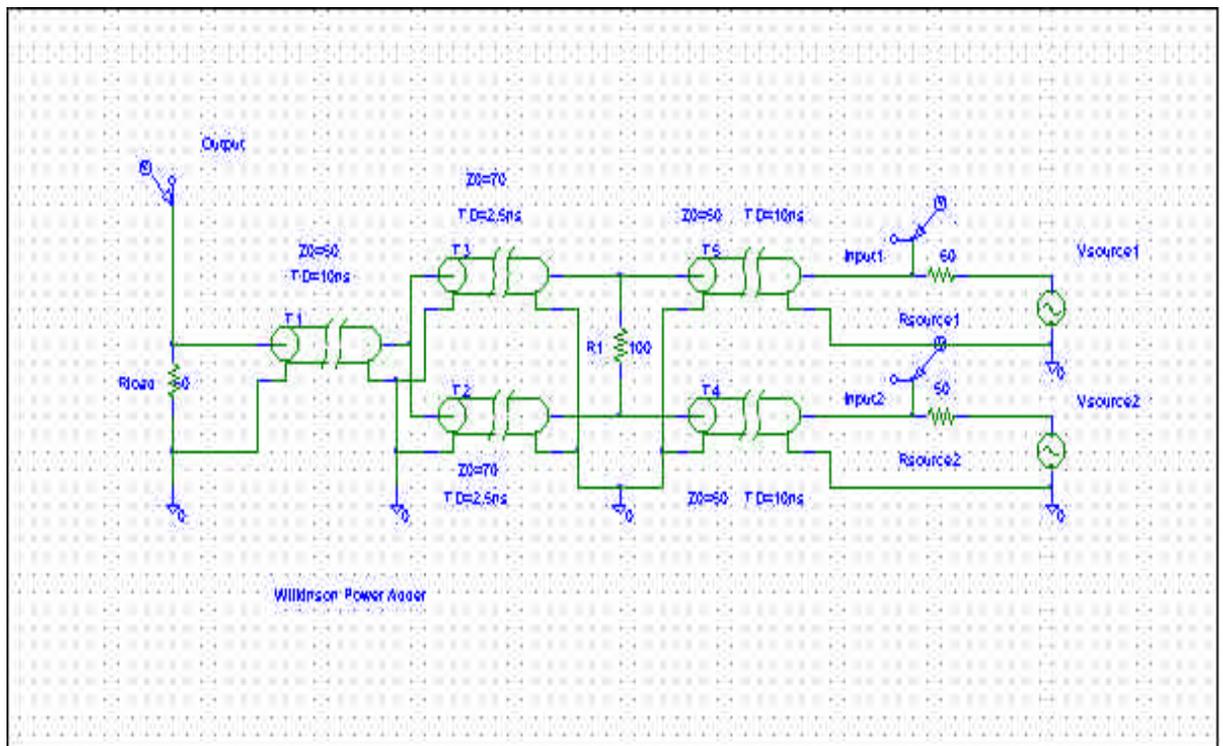
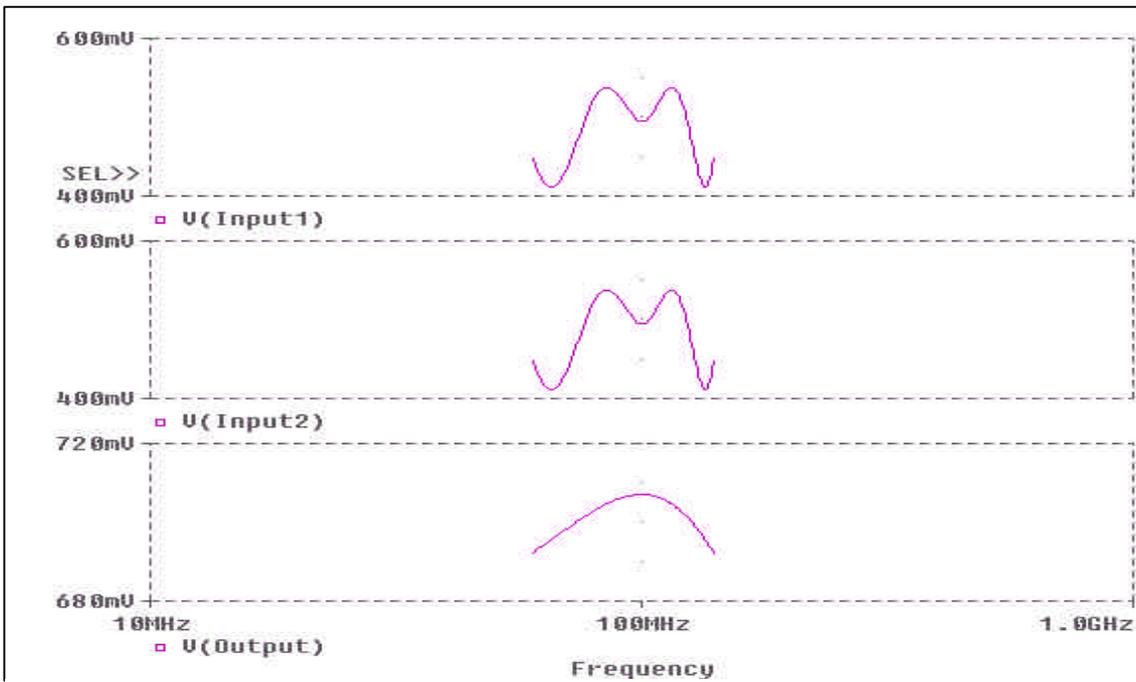
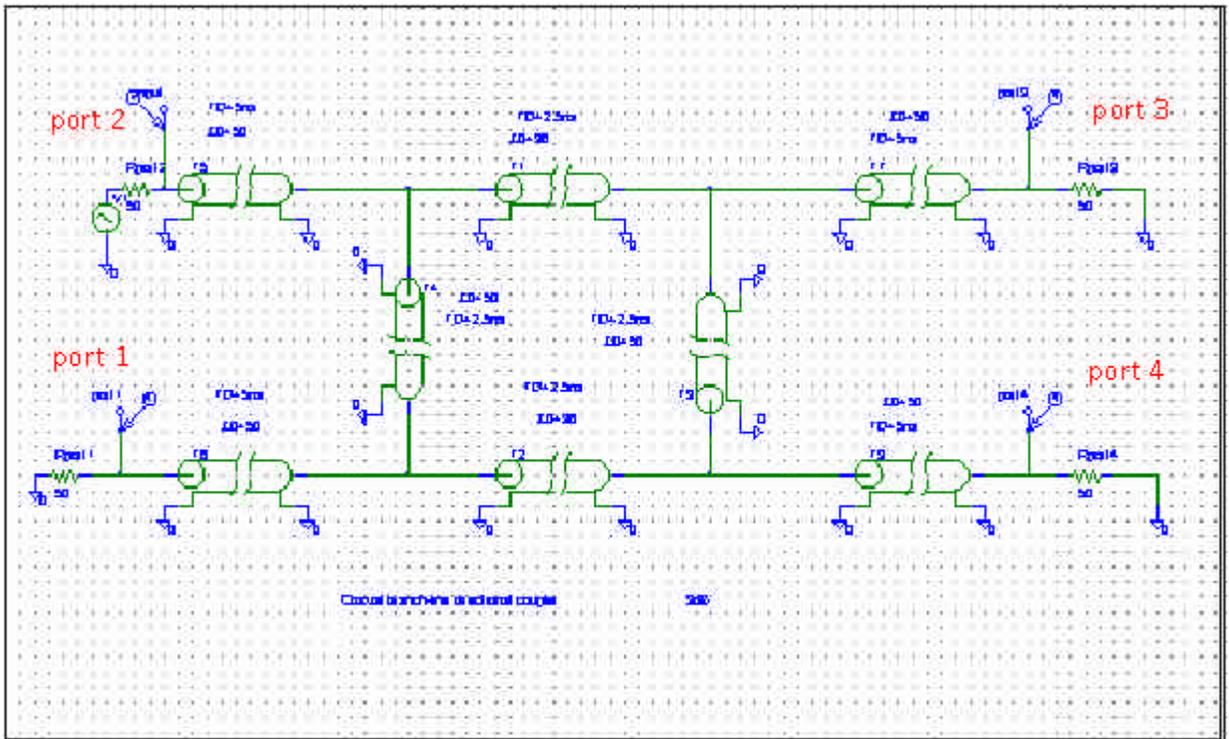


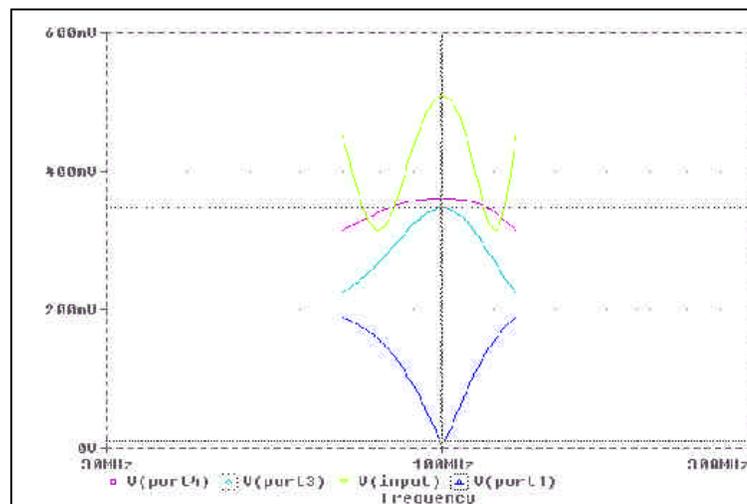
Figure 18: Wilkinson power adder.



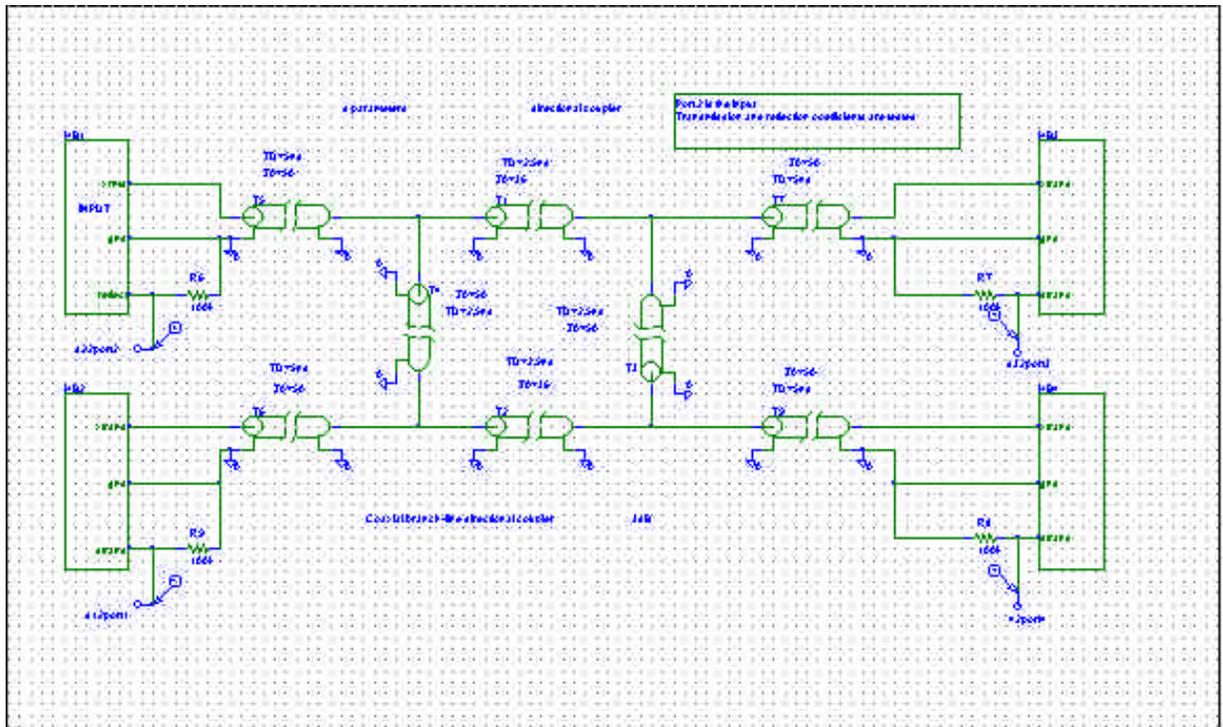
**Figure 19:** Voltages of the Wilkinson power adder as a function of frequency.



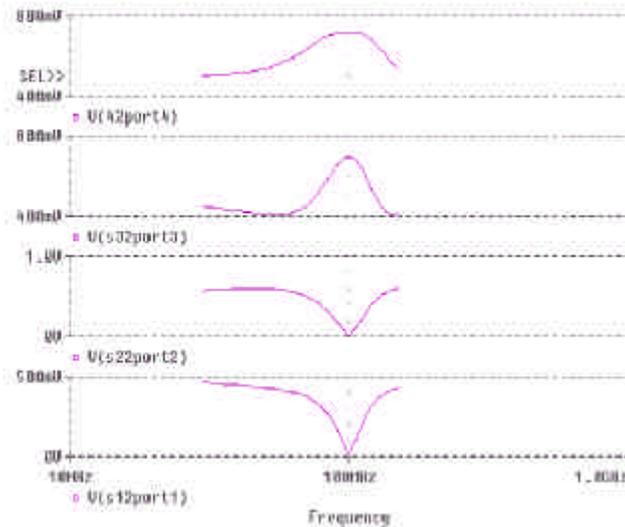
**Figure 20:** PSpice schematic emulation of a directional coupler designed to operate at 100 MHz.



**Figure 21:** Voltage outputs at the ports of the directional coupler as a function of frequency.



**Figure 22:** The circuit shown above is used to obtain the reflection and transfer functions for the directional coupler.



**Figure 23:**  $S_{42}$  and  $S_{32}$  show the forward transfer functions, while  $S_{12}$  indicates the reverse transfer function—the coupler directivity indicator or rejection factor.

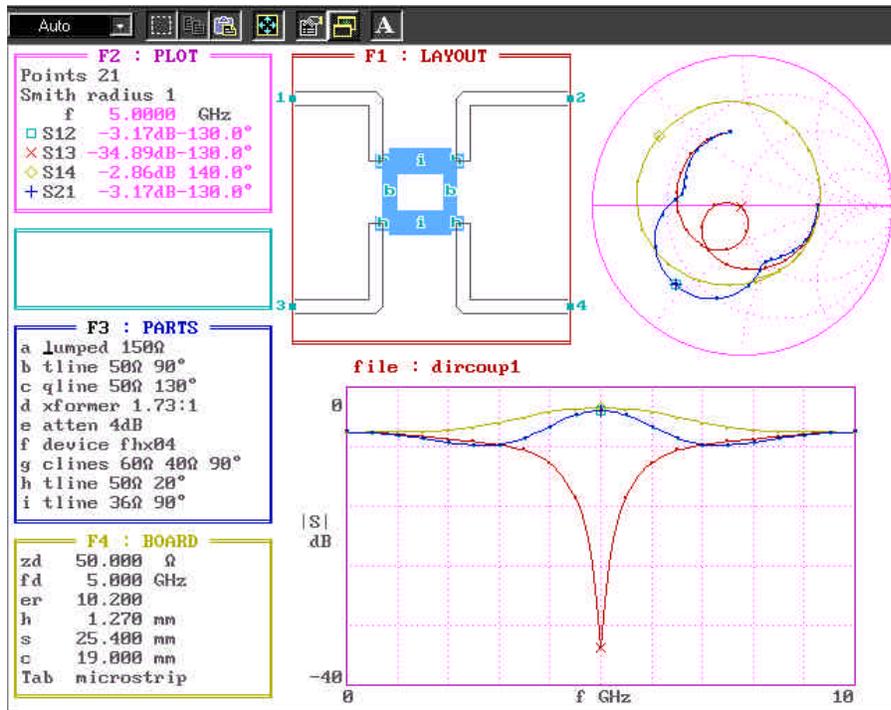


Figure 24: PUFF version of the directional coupler.

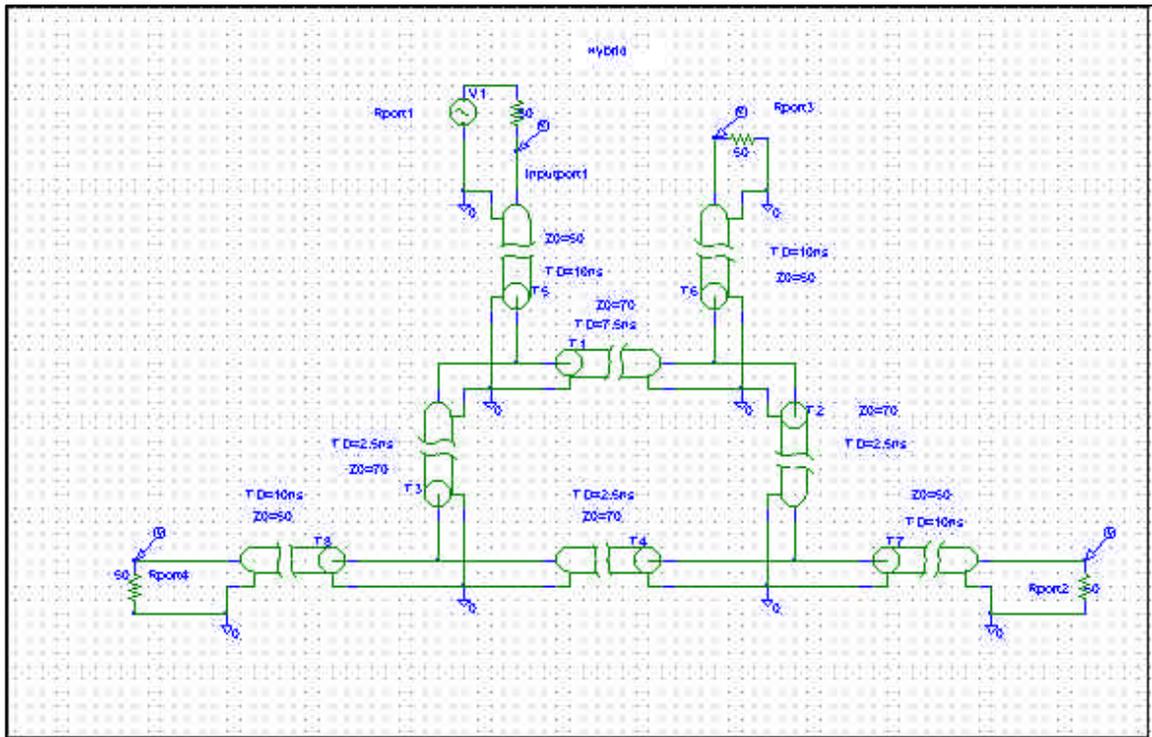
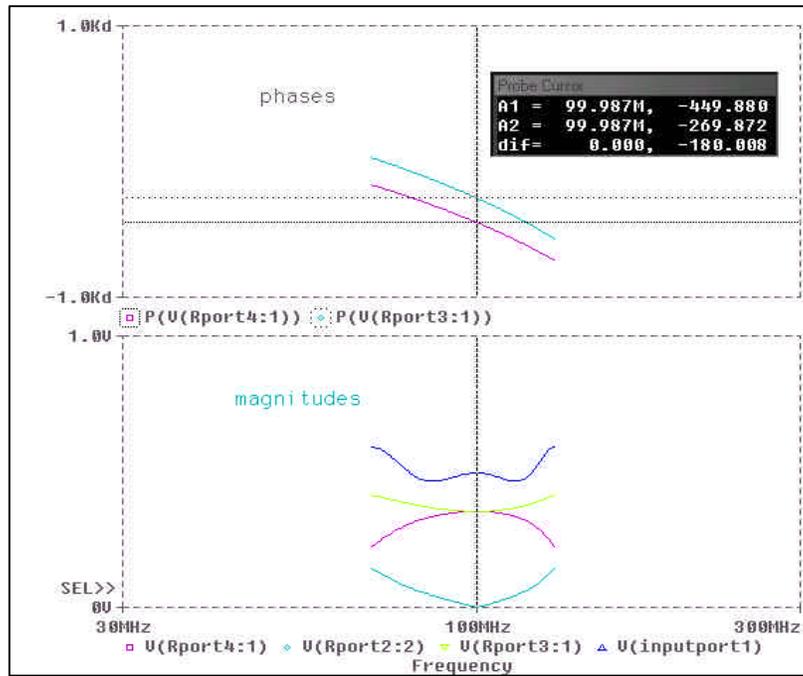


Figure 25: Schematic for the rat-race circuit (ring hybrid).



**Figure 26:** Voltage outputs affiliated with the rat-race schematic of Figure 25.

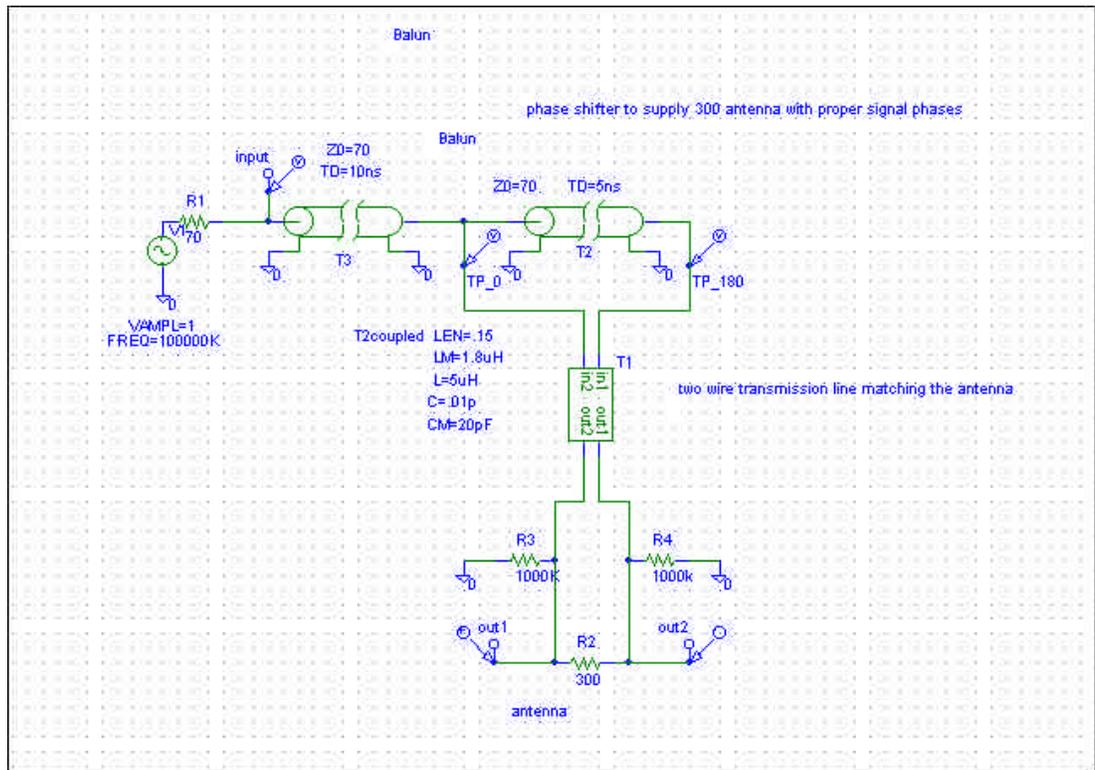


Figure 28: Schematic model for a balun.

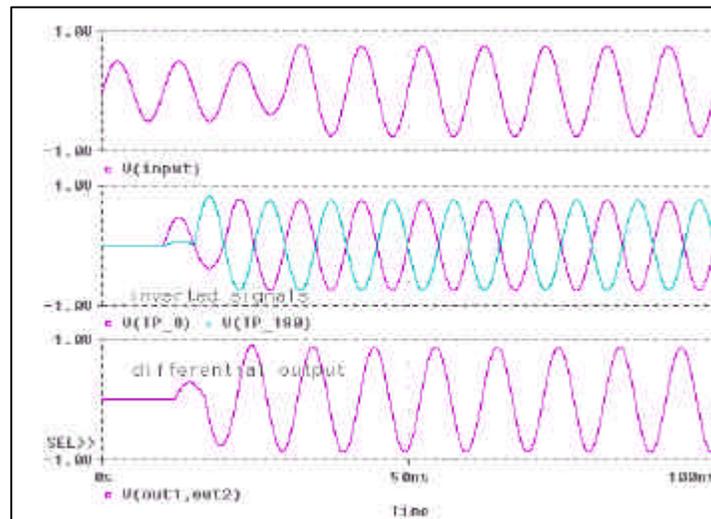
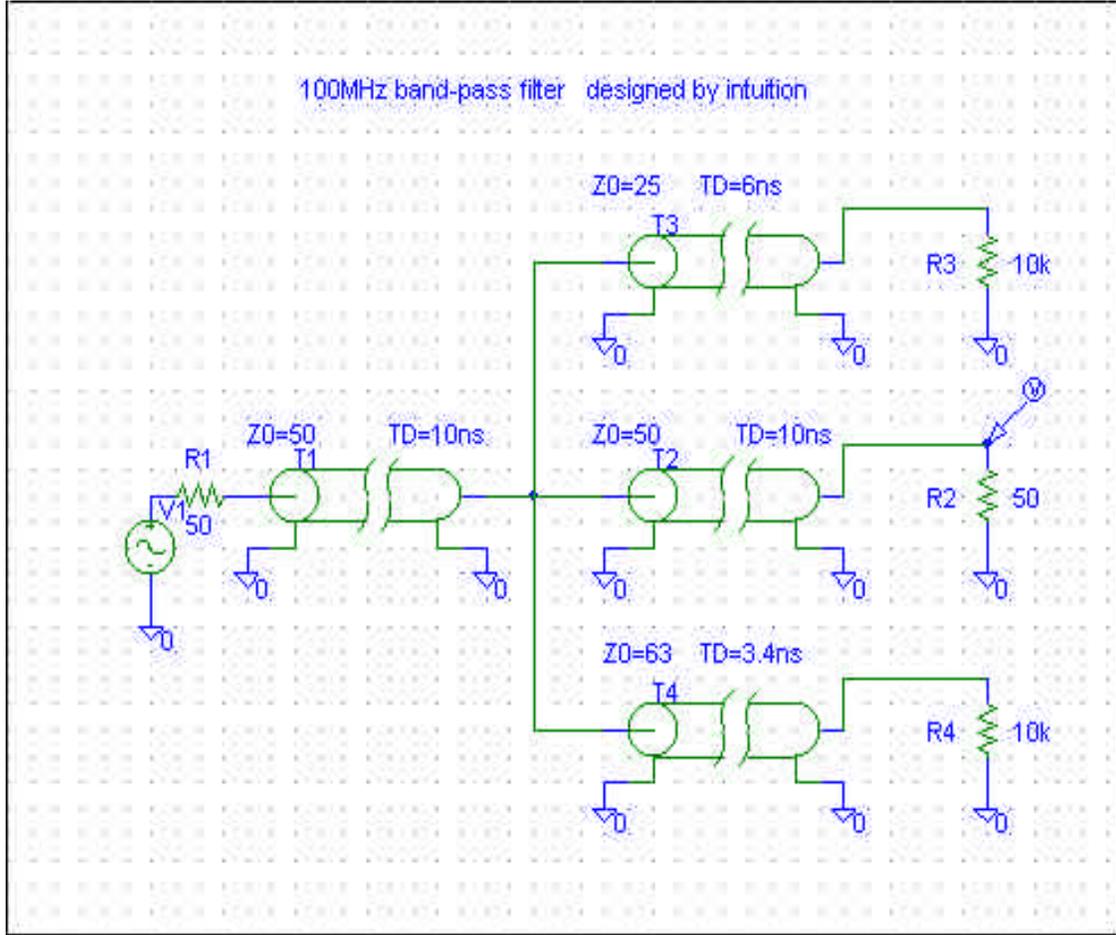
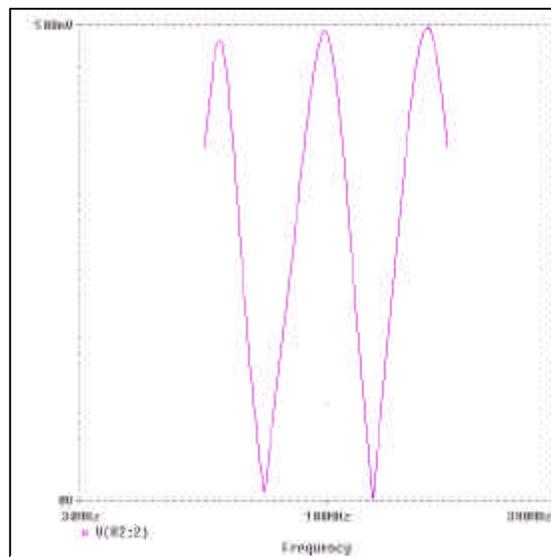


Figure 29: Waveforms affiliated with the balun.



**Figure 30:** Bandpass filter.



**Figure 31:** Frequency spectrum of Bandpass filter.

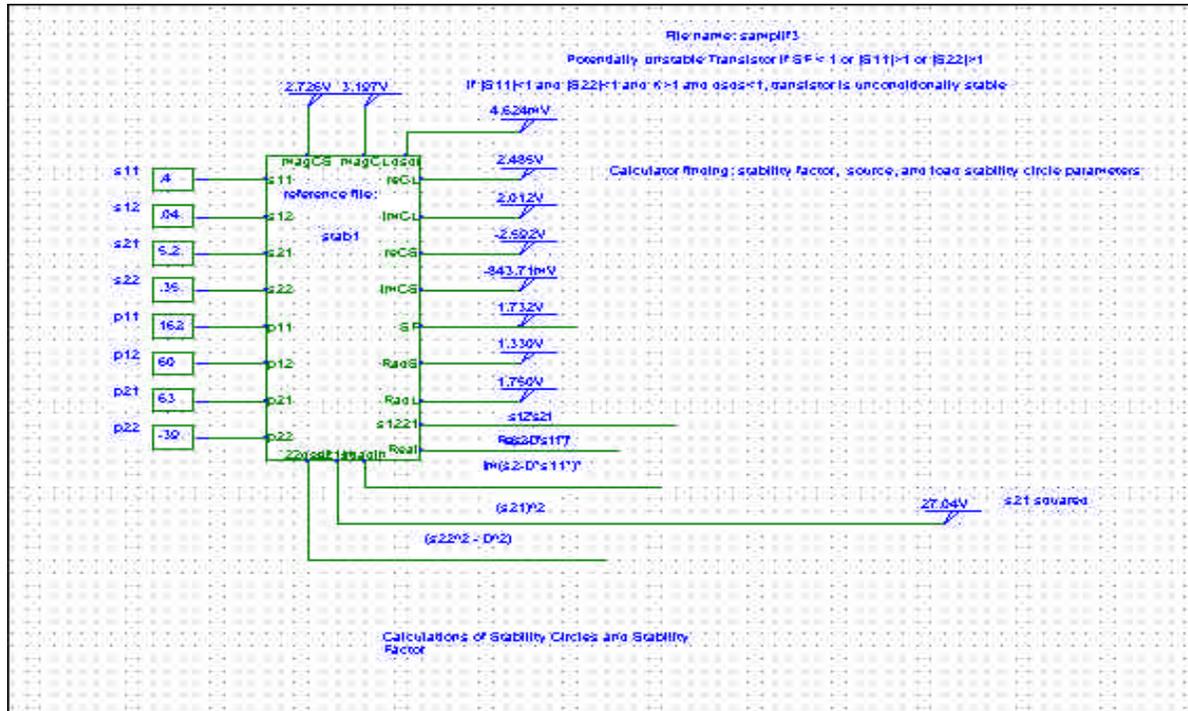


Figure 32: Schematic illustrating Calculator I.

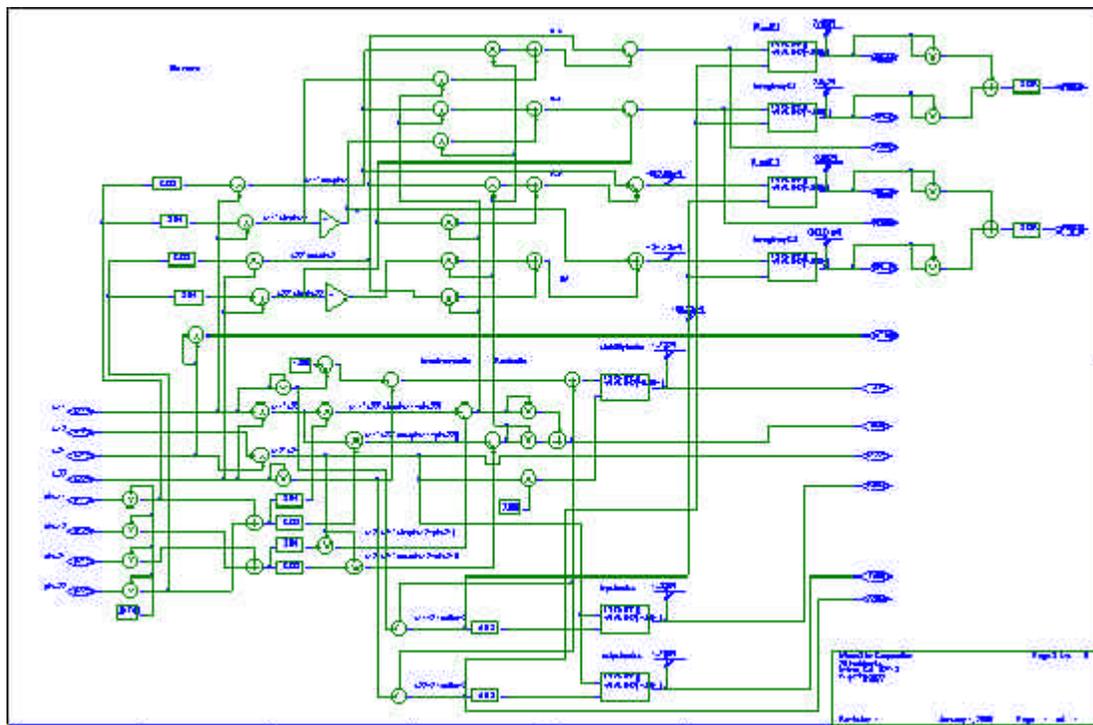


Figure 33: Schematic showing interior of the Calculator I block shown in Figure 34.

## References

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