Performance Comparisons of Modern Digital Signal Processing VLSI Microprocessors

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Abstract *- The continual and rapid evolution of modern DSPuP (Digital Signal Processing microProcessors) makes it difficult for experienced DSP analysts to keep up with technological advances. It is even more difficult for new aspiring analysts to enter the DSP field and try to keep up with evolving technologies. Thus, the authors present reviews and performance comparisons of the newest multiprocessor VLSI DSPuP with the intention of providing concise focused analyses that may help established or aspiring DSP analysts evaluate the applicability of new DSP technology to their specific applications. The Analog Devices SHARC™ and the Texas Instruments TMS320C80 families of DSPuPs will be emphasized with some reference to other processors offered where appropriate.*

1. Introduction

The combination of continually advancing DSP*u*P hardware and constantly evolving DSP algorithm development have formed the basis for an exponential growth in successful DSP applications. The market growth for these applications has resulted in the development of new multiprocessor DSP*u*P VLSI components with very powerful capabilities and complicated operations. It is time consuming for experienced DSP analysts to review and evaluate these new DSP*u*Ps. Aspiring analysts who wish to enter the DSP field would find it even more time consuming, and possibly very difficult to appreciate the significance and opportunities for these new components. Thus, performance comparisons of modern multiprocessor VLSI DSP*u*Ps will be presented in hopes of providing brief time-saving reviews for analysts who need to consider these devices for critical new applications.

The performance comparisons will emphasize the Analog Devices SHARC™ and the Texas Instruments TMS320C80 families. The Motorola DSP96002 and Texas Instruments TMS320C40 will also be considered since the architectures of these microprocessors tend to be well suited for connection with other DSP*u*Ps creating new multiprocessor systems.

Initially, distinguishing architectural features of each of the microprocessors are discussed. Common processor features are then compared and presented in tabular form. The processing speed and power of each of the DSP*u*Ps will then be evaluated in terms of some common digital filtering operations. It should be noted that the digital filtering operations presented were not chosen as a basis for performance criteria because of their implementation and computational complexities. Instead, the operations were chosen due to the fact that they characterize performance criteria common to almost all DSP applications. Finally, evaluations and conclusions relative to performance and applications will be presented.

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2. Modern Parallel DSP*u*P Candidates and Features

The Analog Devices ADSP-21060 SHARC™(Super Harvard Architecture Computer) is a 32-bit processor that builds on the ADSP-21000 core to form a complete system on a chip. It integrates the ADSP-21020, the fastest 32-bit IEEE floating point DSP, with 4 megabits of on chip SRAM to form a powerful computational system. The ADSP-21060 on chip memory represents the largest on chip memory available an any available DSP*u*P. The processor's on chip DMA controller along with it's dual ported memory enables efficient data and instructions transfers by allowing simultaneous memory accesses by both the DMA controller and the core processor.

The ADSP-21060 serial and parallel communications ports combine with the host port and multiprocessor interface to increase the connectivity of the SHARC™ and therefore make it better suited for multiprocessing. In addition to the host port and multiprocessor interface, the ADSP-21060 also features six 4-bit link ports that provide additional I/O and multiprocessing capabilities. Because the bit capacity of the ports are small, these links ports can be clocked more than once per instruction cycle to achieve higher data transfer
rates[DSPA94].

The Texas Instruments TMS320C80 DSP*u*P is actually 5 separate processors integrated together on a single chip. The 5 processors consist of a single master processor and 4 slave parallel processors. The TMS320C80 Master Processor(MP) is a 32-bit, IEEE-754 compatible floating point processor. The MP manages the functions of all components within the chip. It is the main supervisor and distributor of tasks withinthe chip and also functions to communicate with external processors and service external interrupts. The 4 other Parallel Processors(PP) are 32-bit integer units. The 4 processor function independently of each other, perform data computations and handle operations associated with image, graphics and audio processing.

The C80 features 50 Kbytes of on-chip RAM and crossbar switching which allows the on-chip memory to be accessed by the PPs, MP and the Transfer Controller(TC). The Transfer Controller is an interface between internal and external memories and is used for cache servicing and data block transfers between external memory and internal SRAM. The C80 also features a Video controller that acts as a dual frame interface between the TMS320C80 and an image and display system. Finally, the C80 architecture includes a JTAG Emulation Interface that lets the user test programs or scan results through in-circuit emulation[TIMA94].

The Motorola DSP96002 was the first 32-bit microprocessor to implement in hardware the IEEE 754-1985 standard for binary floating point arithmetic. It features a 4 GW(gigaword), where one word is 32 bits, program address space and two 4 GW data address spaces expansion capabilities. Two complete sets of 32-bit buses or ports are provided for external interfacing. The DSP96002 includes 1 KW (kiloword) of program RAM, 1 KW of data RAM, 1 KW data ROM, a dual address generation unit, and a dual-channel DMA(direct memory access) controller[GEOR92].

The DSP96002 also provides a Host MPU/DMA Interface for each of its external bus interface ports. Each Host Interface can be configured as a 8-, 16-, 24-, or 32-bit wide parallel port which may be connected directly to the data bus of a host processor[MOTO89].

The Texas Instruments TMS320C40 features six communications ports for high speed interprocessor communication. Each communications port allows for simple processor to processor communication while it's bi-directional transfers help to maintain maximum communications flexibility. The C40's six channel DMA coprocessor alleviates the CPU of burdensome I/O operations and thereby maximizes

sustained peak CPU performance. The DSP*u*P CPU contains a 40/32-bit floating-point/integer multiplier for high performance in computationally intensive algorithms and includes single cycle IEEE floating point conversion for interface with IEEE-compatible processors.

Two identical external data and address buses support shared memory systems and single cycle data transfers from low speed or high speed memories. Internal TMS32C40 memory includes a 512 byte instruction cache and a combined 8 Kbyte of dual access program or data RAM[TI4093].

The following table summarizes some of the key features of the DSP*u*Ps under consideration. It should be noted that several of the microprocessors actually represent families of processors and therefore have the option of varying processor speeds. In such cases we consider the processor with the highest clock rate and therefore compare the highest peak performances provided in the literature for each processor.

Digital signal processors are designed to perform the multiply and accumulate operations very efficiently since these operations are most prevalent in DSP applications. The processors under discussion take one instruction cycle to perform a single precision multiply or a floating point add. The table below indicates the fastest instruction cycle times found for each of the processors

	TMS32C40	DSP96002	TMS320C80	ADSP21060
DIVIDE	225ns	525ns	125ns	150ns
PRECISION	32bits	32bits	32bits	32bits
RAM/ROM	8.5Kbytes	8Kbytes	50Kbytes	4Mbytes
I CYCLE TIME	25ns	75ns	25ns	25ns

3. Complex FFT Evaluations

The evaluations of DFTs(Discrete Fourier Transforms) with complex FFTs(Fast Fourier Transforms) is such an important component of DSP applications, most DSP*u*P manufacturers include FFT performance data. The following discussion presents the performance of all the DSP*u*Ps in terms of their complex FFT evaluation times of the 1024 point FFT. Where required, manufacturers data values were interpolated using the following equation:

$$T_{PROC} \propto N \log_2 N$$

where

T_{PROC} is defined as the processing time

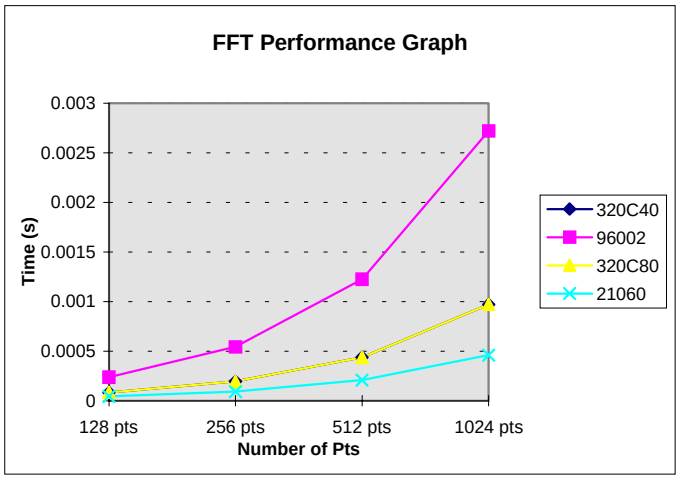
and

N is defined as the number of points to be processed.

Using ratios of the two relevant proportions as a function of *N*, the following values are obtained.

	TMS32C40	DSP96002	TMS320C80	ADSP21060
1024 pts	.97ms	2.72ms	.97ms	.46ms
512 pts	.4365ms	1.224ms	.4365ms	.207ms
256 pts	.194ms	.544ms	.194ms	.092ms
128 pts	.085ms	.238ms	.085ms	.04225ms

Graphically the data can be viewed as follows:

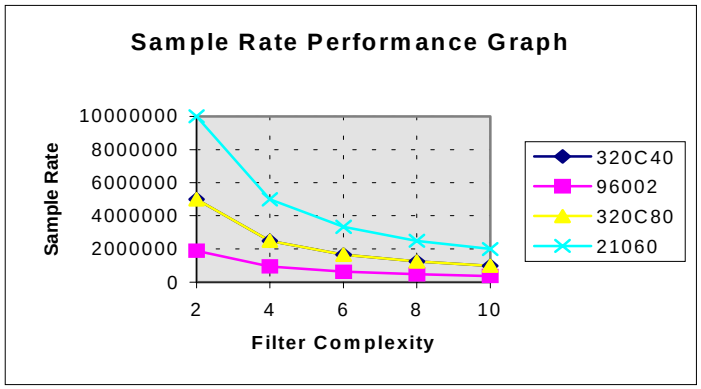


4. IIR Filter Implementations

The next discussion will evaluate the performance of the processors in terms of IIR filter evaluations. The times for biquad evaluation completion were supplied by the manufacturer. Neglecting overhead, higher order filter implementation times may be interpolated from the given data by observing that they are linear functions of the biquad implementation times.

Processor	Biquad Time
ADSP21060	100ns
TMS320C80	200ns
DSP96002	525ns
TMS320C40	200ns

Using the IIR filter implementation times listed above, maximum sample rates for each of the processors may be calculated. The calculated sample rates for IIR filters up to 10^{th} order are presented below in graphical form.



The data represented in the data tables and graph were obtained from the user manuals and data sheets of the individual processors. All of the processors except the DSP96002 assume a 25ns instruction rate. The DSP96002 user manual specified a 75ns instruction rate for FFT evaluation and IIR filter implementation. Because of the differences in specified instruction completion times, the DSP96002's performance evaluation is probably lower than it should be when compared to the others.

The significance of the performance graphs is best understood in terms of some simple illustrations. For example, the number of points in an FFT evaluation will determine the DSP*u*P evaluation time. The FFT evaluation time must not exceed the allotted time for transform completion in each DSP system algorithm sample time; i.e., the time to complete one cycle of all operations for a particular system DSP system. Thus, an analyst must be able to partition all DSP system functions and complete the evaluations within the allotted times - otherwise the proposed system design is not feasible.

For a second example, consider designing an IIR 10^{th} order filter. Performance curves immediately indicate a maximum sample rate achievable by a DSP*u*P. If the filter bandwidth-to-sample frequency implies the DSP*u*P cannot meet the processor speed requirements, then another processor or multiple processors must be considered as alternatives to meet design specifications.

5. Parallel DSP*u*P Application Considerations

The previous sections of discussion sought to evaluate the relative performance of the different micro-processors under discussion by comparing the processing speeds of several operations prevalent in DSP applications. Using these differences in performance along with the differences in key processor features, ideal applications for each of the DSP*u*P may be identified. Since the newer processors tend to have obvious advantages in speed of operation, internal memory capacity and data transfer rates, other issues such as amount of parallelism needed, system cost or problem complexity may also be considered. If these considerations are added in the problem definitions, uses for older processors may be defined.

Video processing will be the first application under discussion. In this paper, the term video processing takes on a broad variety of applications such as video conferencing, document imaging processing, image recognition, multimedia etc. The performance of these applications on a specific processor may be enhanced by efficient implementation of certain algorithms. For example, the numerous algorithms contained in the H.320 standard for video conferencing would gain from faster algorithm implementation. The standards for motion video applications(MPEG1) and still-image video applications(JPEG) would also benefit. The TMS320C80 has the most features suited for video applications. The TMS320C80 virtually offers everything needed for audio and video implementations. The MP of the TMS320C80 can be used to process high precision audio data and 3-D graphics transforms while the four PP's could be used for JPEG implementations, discrete cosine transforms, convolutions etc. Used together they can accomplish polygon shading, MPEG1 audio/video encode and video and audio compression and decompression.

In addition to the 5 processors included in the C80 system, it also has a video controller which aids in audio and video system interface. This is an architectural feature not included in the other processors under discussion and therefore supports the choice of the C80 for video applications. Included in the VC are two identical frame timers with independent asynchronous clocks. Each timer may be used for either video display or capture. Connected to these clocks are two display/capture regions. These two regions are also inside the VC and are controlled by a serial register transfer controller.

It should be noted that the recommendation of the TMS320C80 for video applications should not imply that the C80 outperforms the other processors in all aspects of video processing. However, the total video system implementation capability of the C80 exceeds that of the other *u*Ps under consideration.

Since most *u*Ps are designed for digital signal processing operations, it can be reasonable stated that all of the processors under consideration perform well for computationally intensive applications. If when choosing a processor for problem solution the major issues are processor speed of evaluation and processor memory, the Analog Devices SHARC™ offers the fastest computational capabilities and memory capacity and would therefore be the best choice from this point of view.
Because of its six I/O ports, the TMS320C40 offers the greatest flexibility in multiprocessor architectural design with respect to hardware flexibility. Thus, three dimensional and fault tolerant architectures would benefit from implementation on the processor because it's many I/O ports allow a high degree of inter-processor communication Therefore, the C40 may be the best choice for DSP applications where the parallel communication capabilities of the processors are vital to system operation.
The Motorola 96002 is a general purpose DSP*u*P. It has relatively good speed when compared with the newest and fastest processor in the discussion and its ease of parallel processing implementations, where the processors are connected in a linear fashion, is comparable to all the processors in the discussion. The processor also has an advantage in cost. It is one of the least expensive of the processors under discussion. The special 96 bit floating point operations offer unique precision capabilities also.

The Motorola 96002 also includes simulation software with "the hooks" required for the simple implementation of multiprocessor architectures. These software tool "hooks" allow the user the ability to perform fine grain simulations of designs without having to incur the expenses of actually building the proposed architecture. Simple C subroutines permit the interfacing of simulated processors with each other. Therefore, for cost effective multiprocessor DSP implementations, the 96002 may be the processor of choice.

6. Conclusions

Although it is not feasible to detail al of the features available in each of the processors, the characteristics outlined in the discussion should give the experienced as well as the aspiring analysts a general idea of what is available in each. In addition to the feature summary presented, the performance comparison should provide a quick overview of the processing capabilities of the *u*Ps under consideration.
Specific conclusions concerning the performance of the DSP*u*Ps that have been discussed are very difficult to formulate. However, several general conclusions can be formulated, some of which are:

1. The developers and manufacturers of the newer DSP*u*Ps have evolved their instruction sets to include general purpose operations to the point that almost any DSP algorithm(existing or undiscovered), can be implemented.

2. The basic performance characteristics of processing speed and precision must be carefully addressed when an application demands processing speeds approaching the upper limit of a target DSP*u*P. The alternative multi-processor architectures may become an issue.

3. The key processing speed evaluations of digital filter and FFT implementations could prove very valuable in the early design stages of choosing a particular DSP*u*P for a specific application. The usual trade-offs of sample rate, complexity, DSP*u*P precision(word-size), and sample to signal frequency ratios must be made[SIMO93].

4. In regards to the DSP*u*Ps discussed, it would seem that:

    a. The SHARC is the fastest and most powerful floating point processor and therefore is better suited for numerically intensive applications.
    b. The TMS320C80 design seems to well suited for most operations associated with video processing.
    c. The TMS320C40 six I/O ports gives this processor the most flexibility in design of multi-processor implementation.
    d. The DSP96002 is a general purpose micro-processor suitable for most DSP applications requiring reasonable precision and speed. Also the software tools that accompany this processor may make it the processor of choice to perform multi-processor operations.

The authors have also identified some applications that seem to be the most appropriate for the specific processors; and, if used in conjunction with the performance tables and graphs provided, they should give the analyst a good indication of the processor that is better suited the particular application.

7. Future Performance Comparisons of DSP*u*Ps

Any performance evaluations performed to aid new analysts in their choice(s) of DSP*u*Ps for specific applications needs to be restricted to those most simple global and generic characteristics required to make a proper choice. The authors have attempted to follow this theme in their presentations of primarily hardware performance features. However, software tools are a critical component of any DSP*u*P-based system design. Almost all newer DSP*u*Ps have the general purpose instructions required to implement almost any DSP algorithm. Thus, a performance evaluation of DSP*u*P-based tools needs to focus on ease of use, processor specific software tools, support(mostly 3rd party) tools, support hardware etc. Thus, any successful attempt to quantify these, mostly qualitative, factors and features should probably be based on carefully conducted surveys(evaluations) solicited from successful DSP*u*P-based systems designers working in the forefront of new applications. Thus, further evaluations(with an emphasis on software support tools) should heavily weight information collected from successful DSP*u*P designers.

8. References

[SIMO93] Simons, F. O. Jr.; George, A. D.; Short, C. W.; and Tait, H. S.; "*Architectural Tradeoffs in Digital*
Dynamic Model Implementations", Proceedings of the TMS320 Educators Conference, Houston, Texas, August 10-12, 1993.

[GEOR92] George, A. D., *Microprocessor-Based Parallel Architecture for Reliable Digital Signal Processing*, CRC Press, Boca Raton, Florida, 1992.

[DSPA94] *DSPatch, Number 29,* Applications Newsletter, Analog Devices Inc., Norwood, Massachusetts, 1994.

[TI4093] *TMS320C40 Users Guide*, Texas Instruments, Houston, Texas, 1993.

[MOTO89] *DSP69002 Users Manual*, Motorola, Phoenix, Arizona, 1989.

[TIMA94] Uncopyrighted Work Presented by Texas Instruments and Marshall in the form of a seminar, 1994

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