Position Detector Project

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A. Introduction

This paper discusses the design of a project used in a second year course of Electrical Engineering Technology at Purdue University. The design reviews material that has been covered in the first few analog courses at the University to help students link their knowledge together.

The project uses a variable capacitor that has a rotating plate. The circuit detects the variation in the capacitor. The block diagram of the design is in Figure 1 below.

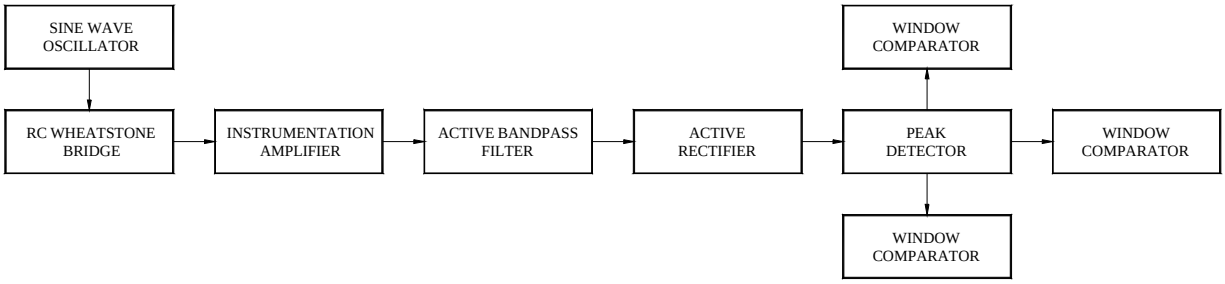

Figure 1 – Block Diagram of the Project

B. The Position Detector Project

1. The Variable Capacitor

The key component of the design is a variable capacitor. It consists of two 8cm by 5cm conduction plates that are place 1mm (0.001m) apart as in Figure 2 on the next page.

The bottom plate is affixed and the top plate rotates about the shaft that results in different plate areas. The capacitance is:

$$C = \frac{A\varepsilon_r\left(8.85\times10^{-12}\,F/m\right)}{d}$$

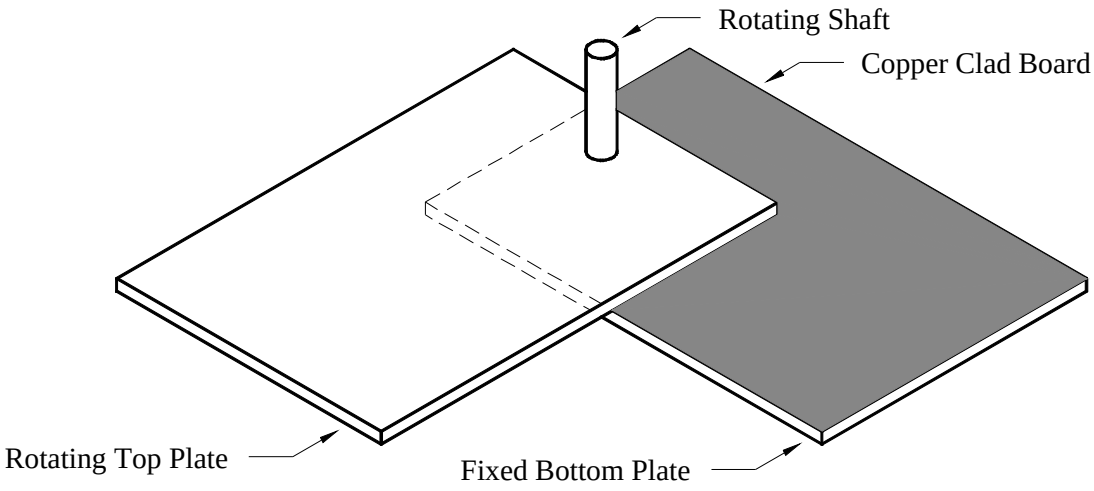

Figure 2 – The Variable Capacitor

In the equation, C is the capacitance in farads, A is the plate area in m^2, e_r is the dielectric constant, and d is the distance between the plates in m. By rotating the top plate, we create a variable capacitor and the design detects this variation.

The plates in this project are double-sided copper clad plates. The two copper sides of each plate are connected together by a wire. When they are 90° apart as in Figure 3, the capacitance is measured to be 95pF.

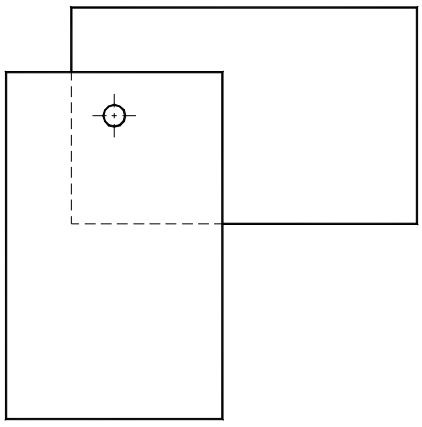

Figure 3 – Top View of the Variable Capacitor

2. The Oscillator

Since the circuit detects the capacitance variation, an ac signal is needed. A sine wave oscillator meets this need and is the first part of our circuit. The schematic diagram of the oscillator is in Figure 4.

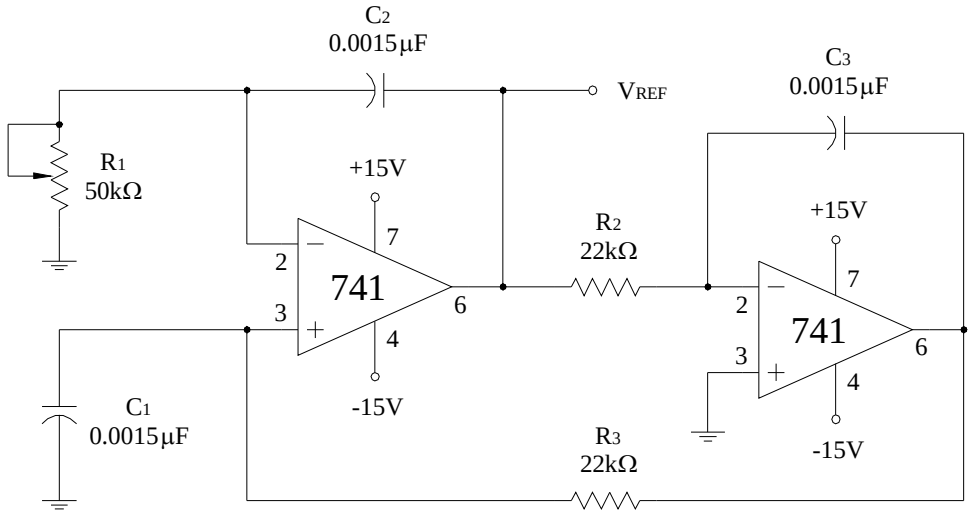

Figure 4 – The Oscillator

Let $R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$, the oscillation frequency is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi(22k\Omega)(0.0015\mu F)} = 4.82kHz$$

In designing the oscillator, the resistors R_2 and R_3 and the capacitors C_1, C_2, and C_3 are matched within 1% of each other. The potentiometer R_1 is a 22-turn trimmer that is tuned so that the circuit oscillates. In our circuit, the value of R_1 is approximately 21kΩ.

The output of the first operational amplifier is a sine wave with its peak value of 15V (power supply voltage) and the output of the second operational amplifier is a cosine wave (90° phase shift) with similar peak value. The waveforms of the output voltages are in Figure 5 on the next page.

The output of the first operational amplifier is used as the reference voltage for the following Wheatstone bridge.

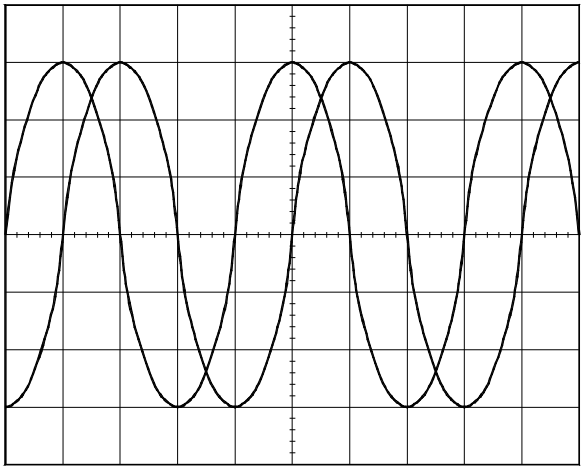

Figure 5 – The Output Waveforms of the Oscillator

3. The Wheatstone Bridge

The schematic diagram of the bridge is in Figure 6 below.

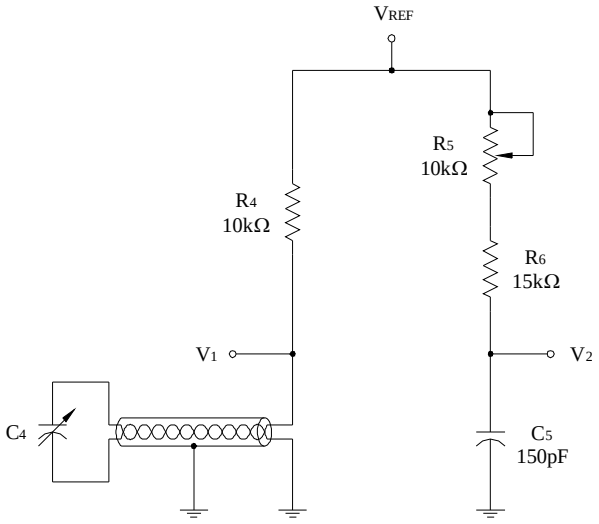

Figure 6 – The RC Wheatstone Bridge

The capacitor C_4 is the variable capacitor discussed previously. When the plates are 90° apart, the capacitance is 95pF. When the rotational plate is on top of the bottom plate, the capacitance is measured to be 150pF. This capacitor is connected to the bridge via a two-conductor shielded

cable. The reference voltage is the sine wave output from the oscillator. This sine wave has its peak value of 15V and frequency of 4.82kHz.

At 95pF, the capacitive impedance is:

$$Z_{C4} = -\frac{j}{2\pi(4.82kHz)(95pF)} = -j347.6k\Omega$$

At 150pF, the capacitive impedance is:

$$Z_{C4} = -\frac{j}{2\pi(4.82kHz)(150pF)} = -j220.1k\Omega$$

With the change of the capacitive impedance of capacitor C_4, the voltage v_1 also changes its peak and phase values.

The other branch of the bridge consists of another series RC network. In order to balance the bridge, the ratios of capacitances and resistances of the two branches of the bridge must be matched. Since C_5 is approximately 1.6 times larger than C_4, the series combination of R_5 and R_6 in the second branch should be 1.6 times larger than R_4. To further fine-tune the balancing of the bridge, a 22-turn 10kΩ potentiometer is connected in series with a 15kΩ resistor to obtain the proper ratio of the resistances in the two branches of the bridge.

The two output voltages of the bridge are used as the inputs of an Instrumentation Amplifier.

4. The Instrumentation Amplifier

The schematic diagram of the Instrumentation Amplifier is in Figure 7 on the next page.

In this amplifier, if we let $R_8 = R_9$, $R_{10} = R_{11}$, and $R_{12} = R_{13}$, the output voltage V_3 is:

$$V_3 = \frac{R_{12}}{R_{11}}\left(1 + \frac{R_8}{R_7}\right)(V_2 - V_1)$$

In the design, the Instrumentation Amplifier has a gain of 31. Note that we must match resistors closely in order for the above equation to be true. In our circuit, R_8 through R_{13} are precision resistors.

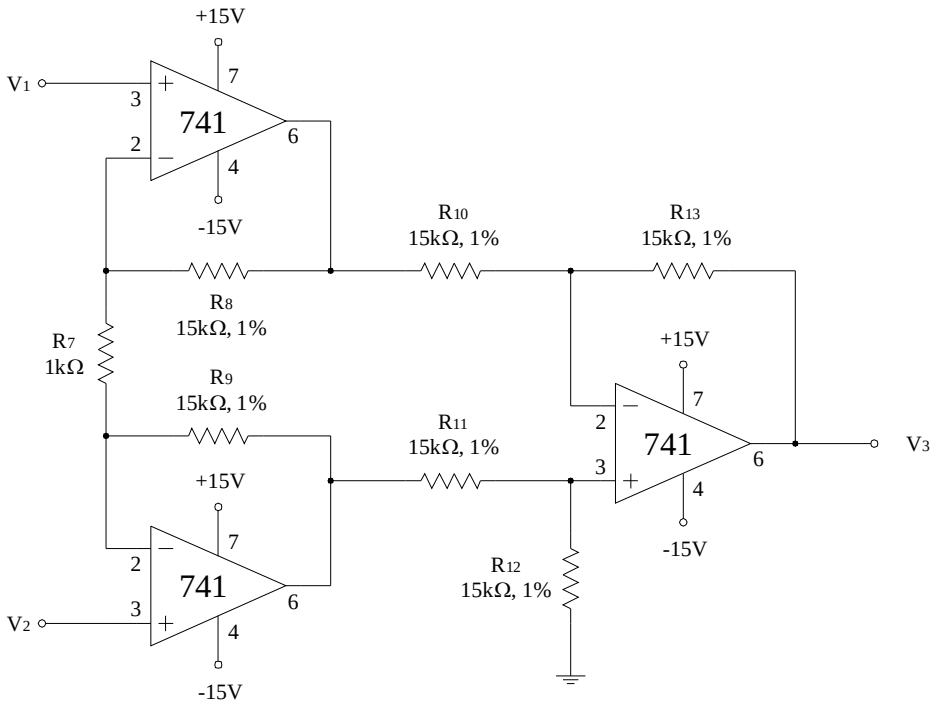

Figure 7 – The Instrumentation Amplifier

The output voltages V_1 and V_2 of the bridge are the input voltages of the amplifier. After connecting the circuit, adjust the potentiometer R_5 to obtain the minimum output of the amplifier when the two plates are 90° apart. Ideally, the output voltage of the Instrumentation Amplifier is zero under these input conditions, but because we are using non-ideal components, our circuit exhibits the waveform in Figure 8. The peak-to-peak value of the wave is approximately 80mV.

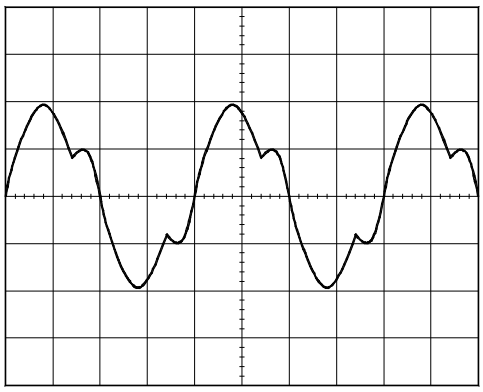

Figure 8 – The Output Waveform of the Instrumentation Amplifier

This wave also rides on a 60Hz signal of 50mV peak-to-peak. This low frequency interference is introduced to the circuit via the connecting cable of the variable capacitor and the power supply unit.

When the two plates are 60°, 30°, and 0° apart, the peak-to-peak values of the output of the Instrumentation Amplifier are 220mV, 360mV, and 520mV respectively.

The output of the amplifier then goes to a Second Order Active Bandpass Filter to amplify the signal more, to condition the signal to produce a perfect sine wave, and to eliminate the 60Hz interference.

5. The Second Order Active Bandpass Filter

The schematic diagram of the filter is in Figure 9 below.

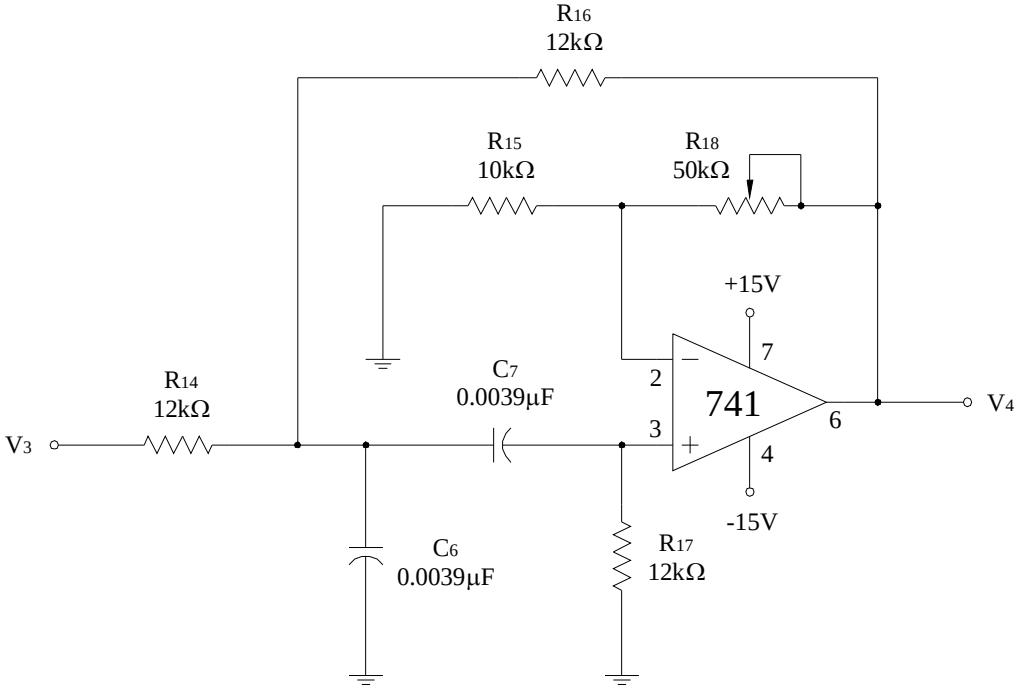

Figure 9 – The Second Order Active Bandpass Filter

In the circuit, if we let $C_6 = C_7 = C$ and $R_{14} = R_{16} = R_{17} = R$, the center frequency is:

$$f_0 = \frac{\sqrt{2}}{2\pi RC}$$

Since the desired center frequency is 4.82kHz, let C be 0.0039μF, then:

$$R = \frac{\sqrt{2}}{2\pi(4.82kHz)(0.0039\mu F)} = 11.97k\Omega$$

We use 12kΩ for R_{14}, R_{16}, and R_{17}.

The Q value of the circuit is: $Q = \frac{\sqrt{2}}{4-K}$

Where K is closed-loop gain of the Noninverting Amplifier section of the circuit. In the filter, the desired value of Q is 10.

$$4 - K = \frac{\sqrt{2}}{10} \Rightarrow K = 4 - \frac{\sqrt{2}}{10} = 3.8586$$

Let R_{15} be 10kΩ, then:

$$R_{18} = R_{15}(3.8586 - 1) = 10k\Omega(2.8586) = 28.586k\Omega$$

A 50kΩ 22-turn potentiometer is used in place of R_{18} and it is set to the desired value. In the design, it is best to use precision resistor for R_{15} because a slight variation of the closed-loop gain could result in a huge change in the Q value.

The output voltage V_4 of the filter now is a perfect sine wave and the 60Hz interference is eliminated.

When the plates are 90° apart, the peak value of the sine wave is:

$$V_{4PEAK} = \frac{V_{3PEAK}(10)(3.8586)}{\sqrt{2}} = \frac{(40mV)(10)(3.8586)}{\sqrt{2}} = 1.1V$$

When the plates are 60° apart, the peak value of the sine wave is:

$$V_{4PEAK} = \frac{V_{3PEAK}(10)(3.8586)}{\sqrt{2}} = \frac{(110mV)(10)(3.8586)}{\sqrt{2}} = 3.0V$$

When the plates are 30° apart, the peak value of the sine wave is:

$$V_{4PEAK} = \frac{V_{3PEAK}(10)(3.8586)}{\sqrt{2}} = \frac{(180mV)(10)(3.8586)}{\sqrt{2}} = 4.9V$$

When the plates are 0° apart, the peak value of the sine wave is:

$$V_{4PEAK} = \frac{V_{3PEAK}(10)(3.8586)}{\sqrt{2}} = \frac{(260mV)(10)(3.8586)}{\sqrt{2}} = 7.1V$$

The sine wave output of the filter then goes into an Active Full-Wave Rectifier to double its frequency to enhance the performance of the Active Peak Detector circuit.

6. The Active Full-Wave Rectifier

The schematic diagram of the circuit is in Figure 10 below.

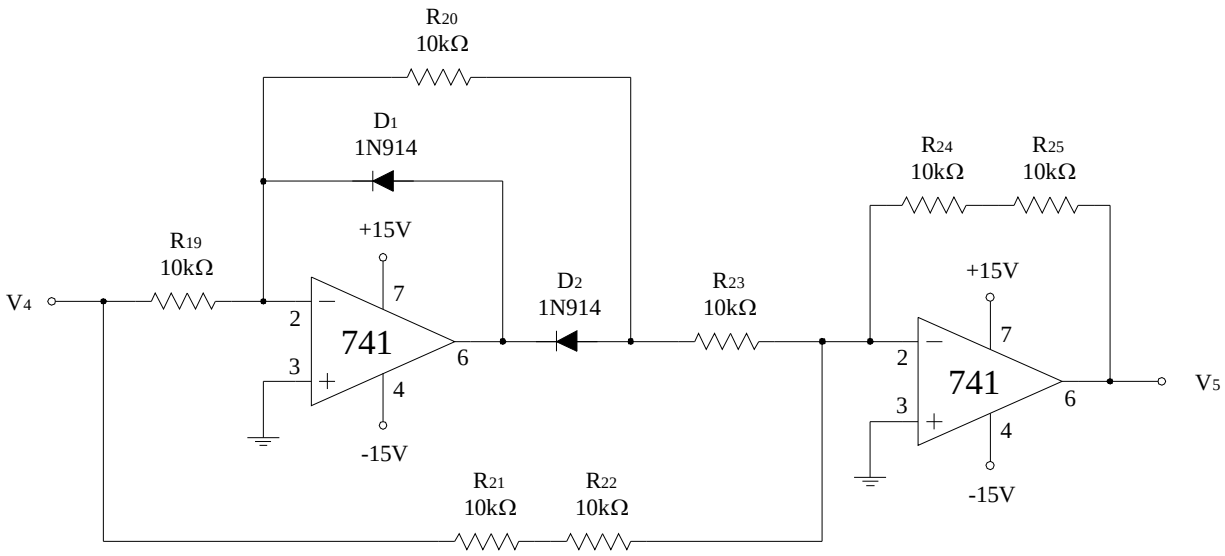

Figure 10 – The Active Full-Wave Rectifier

To study the behavior of the circuit, we will investigate its response during different half cycles of the input voltage.

During the positive half-cycle, the diode D_1 is reverse biased and the diode D_2 is forward biased. The equivalent circuit is in Figure 11 on the next page.

The first section of the circuit is an Inverting Amplifier. If we let $R_A = R_B$, the voltage V_X is:

$$V_X = -\frac{R_A}{R_B}V_{IN} = -V_{IN}$$

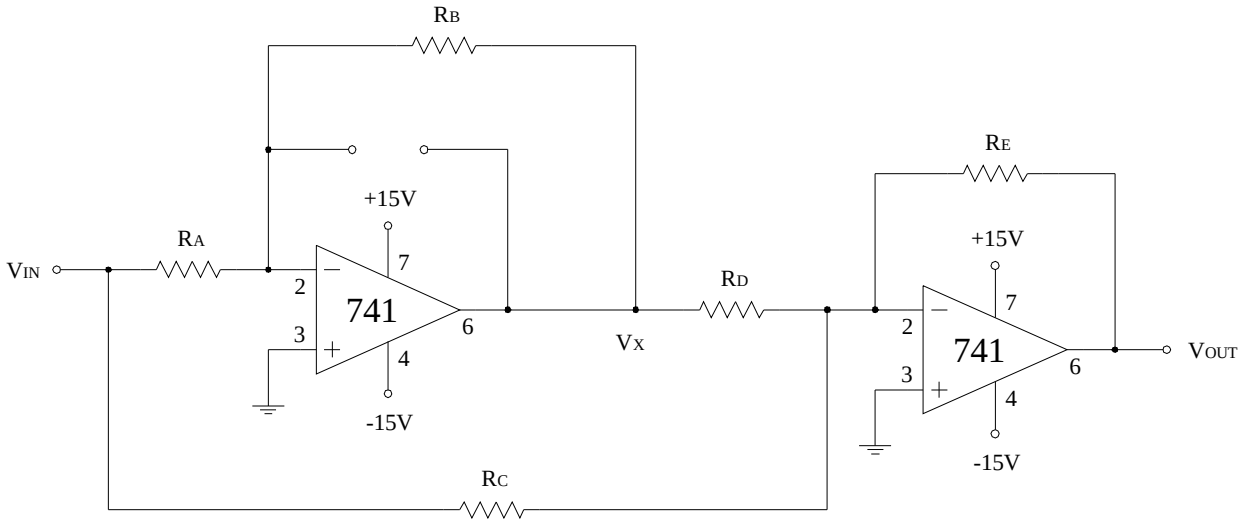

Figure 11 – The Equivalent Circuit During the Positive Half-Cycle

The second section of the circuit is a Summing Amplifier. The output of this amplifier is:

$$V_{OUT} = -R_E\left[\frac{V_X}{R_D} + \frac{V_{IN}}{R_C}\right] = -\frac{R_E}{R_D}\left(-V_{IN}\right) - \frac{R_E}{R_C}V_{IN}$$

If we let $R_E = R_C = 2R_D$, then: $V_{OUT} = 2V_{IN} - V_{IN} = V_{IN}$

Therefore, during the positive half-cycle, the output voltage is equal to the input voltage.

During the negative half-cycle, the diode D_1 is forward biased and the diode D_2 is reversed biased. The equivalent circuit during this half-cycle is in Figure 12 on the next page.

The voltage V_X in this case is 0V (virtual ground). The second section of the circuit is still a Summing Amplifier. The output of this amplifier is:

$$V_{OUT} = -R_E\left[\frac{V_X}{R_B + R_D} + \frac{V_{IN}}{R_C}\right] = -\frac{R_E}{R_C}V_{IN} = -V_{IN}$$

Therefore, during the negative half-cycle, the output voltage is equal to the inverse of the input voltage.

The input and output waveforms of this circuit are in Figure 13 on the next page.

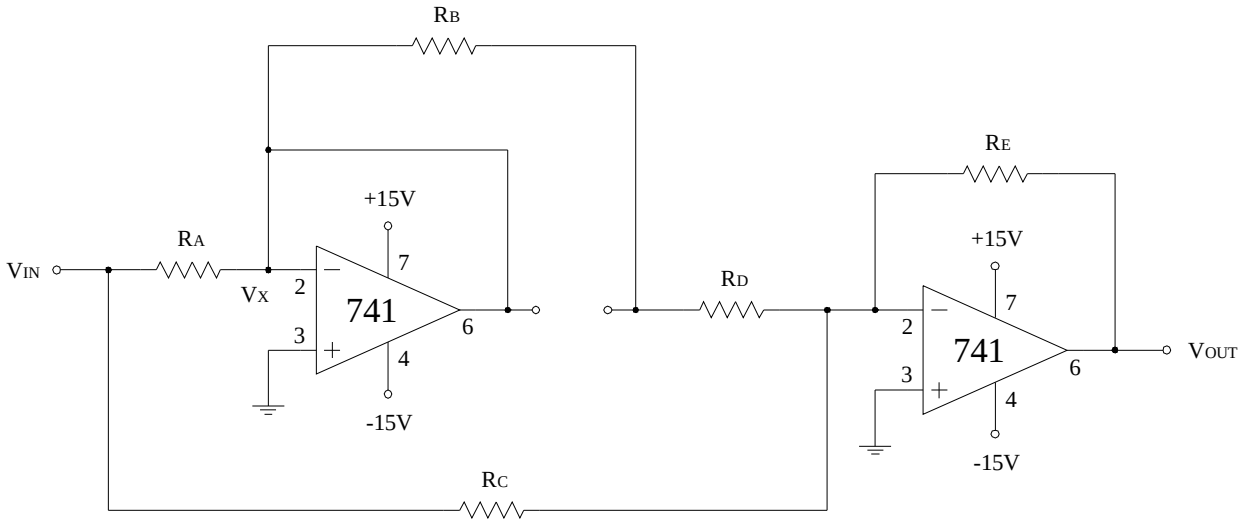

Figure 12 – The Equivalent Circuit During the Negative Half-Cycle

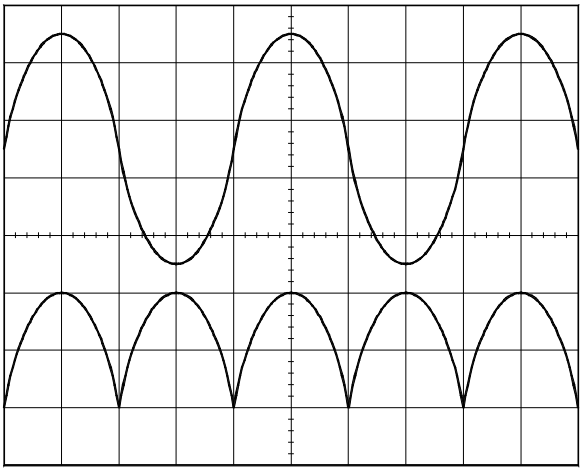

Figure 13 – The Input and Output Waveforms

In our circuit, we use series resistors (R_{21}-R_{22} and R_{24}-R_{25}) to satisfy the resistance requirements as discussed previously. The output frequency of this circuit is 9.64kHz.

7. The Active Peak Detector Circuit

The pulsating DC signal is converted into a DC signal by the Active Peak Detector circuit.

The schematic diagram of the circuit is in Figure 14 on the next page.

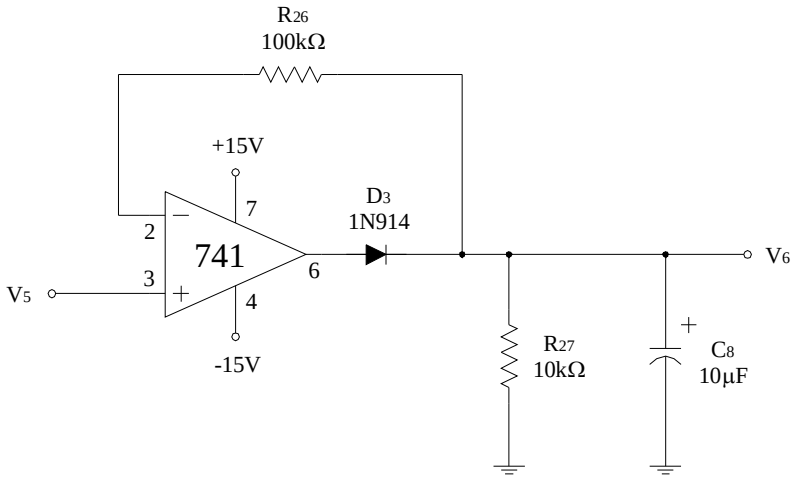

Figure 14 – The Active Peak Detector Circuit

In the circuit, if the R_{27} and C_8 time constant is a lot larger than the period of the input wave, the wave is "smoothed out" to become an almost DC voltage. This voltage has a small ac ripple.

The time constant of the circuit is: $\tau = (10k\Omega)(10\mu F) = 100ms$

And the period of the input wave is: $T = \dfrac{1}{9.64kHz} = 103.7\mu s$

The typical waveforms of the input and output voltages are in Figure 15 below.

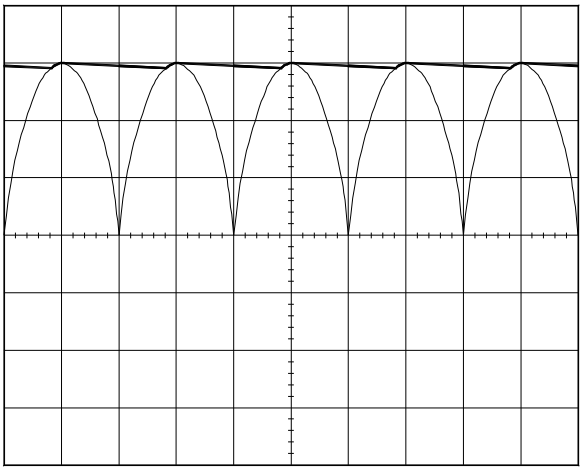

Figure 15 – The Typical Input and Output Waveforms

When the output of the Active Full-Wave Rectifier circuit is at its maximum of 7V, the DC current in the Active Peak Detector Circuit is:

$$I_{DC} = \frac{7.1V}{10k\Omega} = 0.71mA$$

And the peak-to-peak ripple voltage is:

$$V_{RIPPLE} = \frac{I_{DC}}{fC} = \frac{0.71mA}{(9.64kHz)(10\mu F)} = 7.4mV$$

The above ripple voltage is negligible compared to 7VDC. Therefore, the output voltages of the circuit are 1.1VDC, 3VDC, 4.9VDC, and 7.1VDC when the plates are 90°, 60°, 30°, and 0° apart respectively.

To this point of the design, we have three different voltage levels that indicate the relative position of the top plate to the bottom plate. These voltage levels are:

- When the plates are from 0° to 30° apart, the voltage is from 7.1VDC to 4.9VDC.
- When the plates are from 30° to 60° apart, the voltage is from 4.9VDC to 3VDC.
- When the plates are from 60° to 90° apart, the voltage is from 3VDC to 1.1VDC.

We use different Voltage Comparator and Window Comparator circuits to produce some indications under the following conditions:

- When the plates are from 0° to 30° apart, a green LED is on.
- When the plates are from 30° to 60° apart, a yellow LED is on.
- When the plates are from 60° to 90° apart, a red LED is on.

8. The Voltage Comparator and Window Comparator Circuits

There are two types of comparator circuit that we can use to serve the above purposes. To drive the red LED, we use the following circuit.

The schematic diagram of the first Voltage Comparator is in Figure 16 on the next page.

In this circuit, we utilize the open-loop gain of the 741 operational amplifier (about 100,000). The output of the circuit is:

$$V_{OUT} = 100{,}000(V_{REF1} - V_6)$$

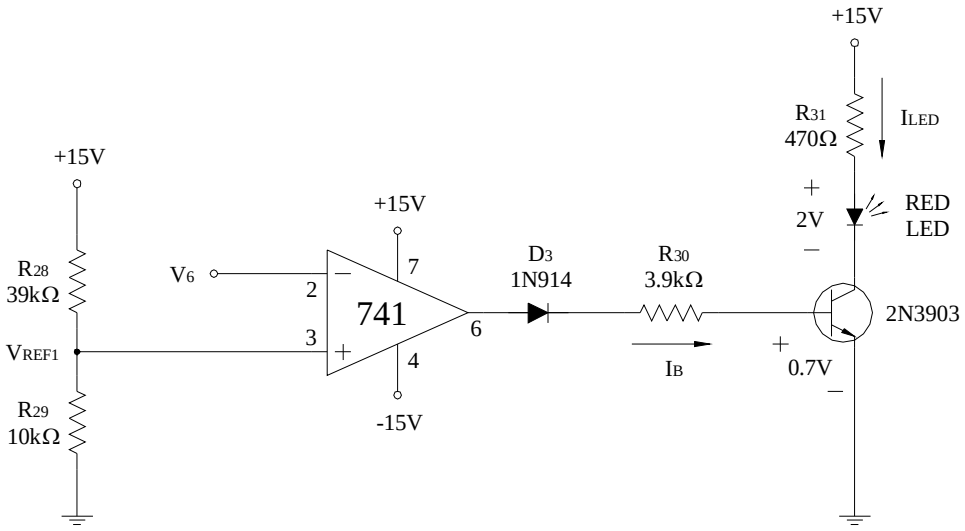

Figure 16 – The Voltage Comparator

When V_{REF1} is larger than V_6, the output voltage of the operational amplifier is positively saturated (about 95% of V_{CC} or 14.25V). When V_{REF1} is less than V_6, the output of the comparator is negatively saturated (about –14.25V).

Since we wish to have the red LED on until V_6 reaches 3V, a voltage divider section consisting of R_{28} and R_{29} is used to produce this reference voltage V_{REF1}.
Let V_{REF1} be 3V and R_{29} be 10kΩ, we have:

$$3V = 15V\,\frac{10k\Omega}{R_{28}+10k\Omega} \Rightarrow R_{28} = \frac{(15V)(10k\Omega)}{3V} - 10k\Omega = 40k\Omega$$

We use a 39kΩ resistor for R_{28}.

We use the output of the Voltage Comparator as the input of a transistor driver to turn on/off the red LED.

The current driving the red LED is 30mA. The resistor R_{31} is:

$$R_{31} = \frac{V_{CC} - V_{LED}}{I_{LED}} = \frac{15V - 2V}{30mA} = 433.3\Omega$$

We use a 470Ω resistor for R_{31}.

In order for the transistor to be in switching mode, let the base current I_B to be 3mA (I_B>10%I_{LED}).

The resistor R_{30} is:

$$R_{30} = \frac{V_{OUT} - V_D - V_{BE}}{I_B} = \frac{14.25V - 0.7V - 0.7V}{3mA} = 4.28k\Omega$$

We use a 3.9kΩ resistor for R_{30}.

Thus, when V_6 is less than 3V, the output voltage of the Voltage Comparator is 14.25V driving the base of the transistor to put it in saturation to turn on the red LED. When V_6 is more than 3V, the output of the Voltage Comparator is –14.25V. The diode D_3 is reverse biased. The transistor is in cut off turning off the red LED.

We can use similar approach to drive the green LED. The circuit is in Figure 17 below.

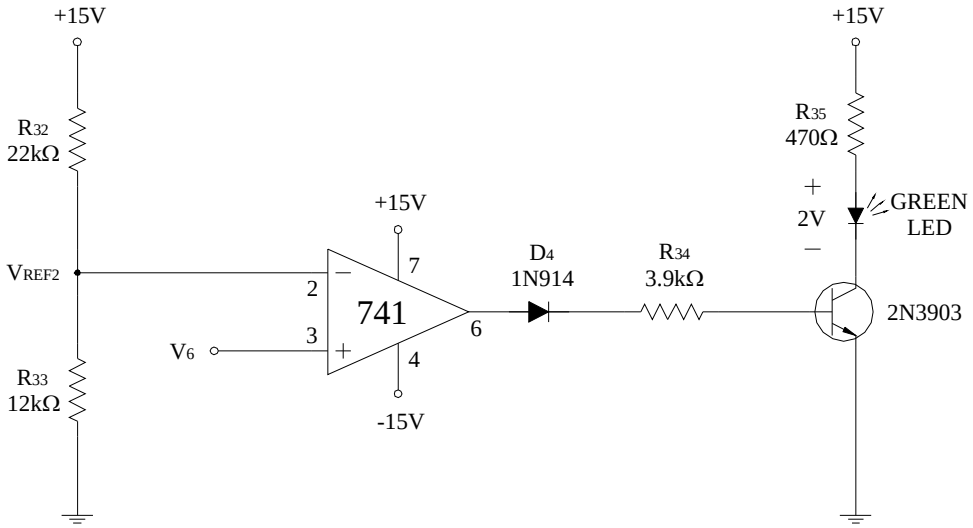

Figure 17 – Another Voltage Comparator

The output voltage of the operational amplifier is:

$$V_{OUT} = 100{,}000(V_6 - V_{REF2})$$

In the circuit, a second reference voltage V_{REF2} is:

$$V_{REF\,2} = (15V)\frac{12k\Omega}{22k\Omega + 12k\Omega} = 5.3V$$

Thus, when the input voltage V_6 is less than V_{REF2} of 5.3V, the output of the Voltage Comparator is negatively saturated turning off the green LED.

When the input voltage V_6 is more than V_{REF2} of 5.3V, the output of the Voltage Comparator is positively saturated turning on the green LED.

We can combine the above ideas to create a Window Comparator circuit to drive the yellow LED. The schematic diagram of this circuit is in Figure 18 below. In the circuit, the reference voltages V_{REF1} and V_{REF2} discussed previously are use as the lower limit and upper limit voltages of the comparator.

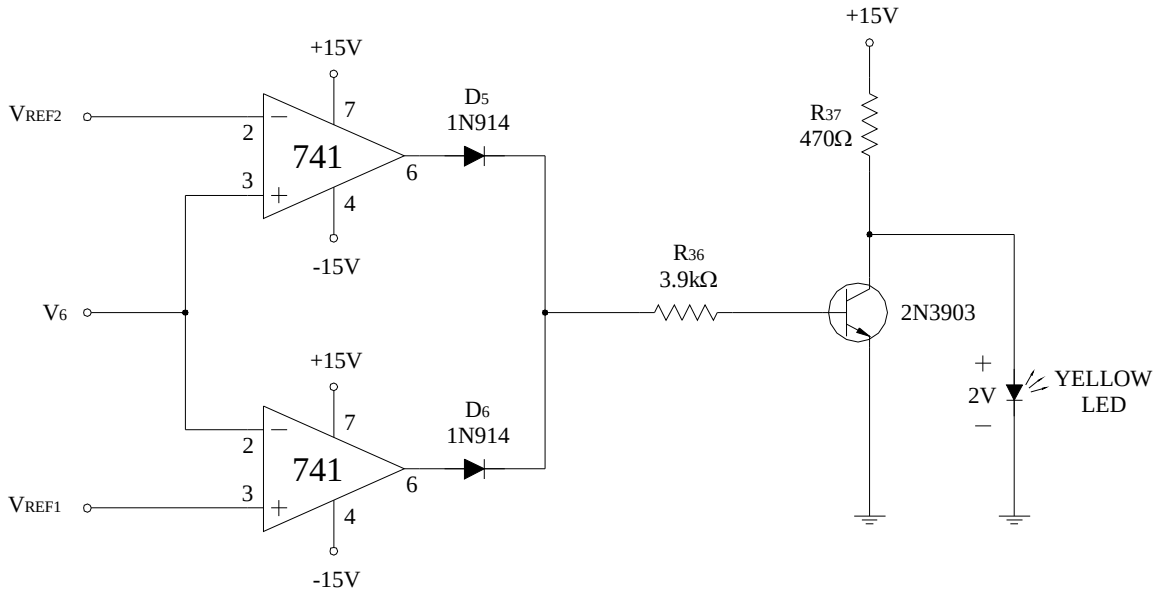

Figure 18 – The Window Comparator

When the input voltage V_6 is more than V_{REF2}, the output of the top comparator is positively saturated. This voltage drives the transistor into saturation resulting in the yellow LED being off.

When the input voltage V_6 is less than V_{REF1}, the output of the bottom comparator is positively saturated. This voltage drives the transistor into saturation resulting in the yellow LED being off.

When the input voltage V_6 is between V_{REF1} and V_{REF2}, the outputs of both top comparators are negatively saturated. This voltage drives the transistor into cut-off resulting in the yellow LED being on.

C. Conclusion

The project produces indicators for the relative position between the top plate and the bottom plate of the variable capacitor. A red LED shows that the two plates are between 60° to 90° apart. A yellow LED indicates that the two plates are between 30° to 60° apart and a green LED indicates that the two plates are between 30° to 0° apart.

The project consists of different analog circuits that the students have learned during the first three semesters in the Electrical Engineering Technology Program of Purdue University. This design gives the students an opportunity to put into practice the theories and applications they possess. It also enhances their troubleshooting skills.

Bibliography

1. Boylestad, R. L. (1995). Introductory circuit analysis (6th ed.). Ohio: Merrill Publishing.
2. Budak, A. (1974). Passive and active network analysis and synthesis. Boston: Houghton Mifflin.
3. Malvino, A. P. (1999). Electronic Principles (6th ed.). Ohio: Glencoe/McGraw-Hill.

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