Preparing Students with Industrial Collaboration in Meeting the Challenges in Engineering Design with Consummate VLSI Education

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Abstract:

For in-depth Microelectronics education, state-of-the-art laboratory facilities are required to complement theoretical instructions in order to validate the modeled microelectronic design from its conception to the finished chip along with its real time testing. University laboratory facilities are utilized for a broad range of microelectronic designs but fabrications of complex devices are not often achieved due to the budgetary/equipments limitations. The system design in general and VLSI system in particular needs multidisciplinary skills. The VLSI education model addresses this problem adequately. In order to become an integral VLSI designer one needs to inculcate skills in design, simulation, testing and verification. This requires a special commitment of funds, which are beyond budgetary allocations of the schools.

The partnership between academia and industry is of vital importance, especially through sponsorship of UMass Lowell's VLSI Design and Fabrication activities. The VLSI program comprises of four distinct and disparate phases namely-Phase 1: Chip design – This basically involves the design of the chip based on specifications provided by the customer, Phase 2: Mask Set – It involves the conversion of design's layout and placement into set of masks e.g. diffusion, contact, and metallization masks etc., Phase 3: Mask Transfer – This involves transferring the mask set onto a wafer substrate such as Si or GaAs etc., Phase 4: Packaged Chip – This incorporates inscribing, dicing, bonding and encapsulating chip in a plastic or ceramic package, depending on customer's requirement. In order to enhance the design capabilities UMass Lowell received a donation of $28m from Cadence and 50% discount from SUN on sparc stations, with a promise to pay $5k to Cadence for license agreement, which is cardinal stone of Phase I since 1998. Phase II has not been achieved yet at UMass Lowell due to budgetary constraints. Phase 3 however, was consummated in its entirety through Distributed Semiconductor Instructional Processing Laboratory (DSIPL), a unique facility established at UMass Lowell in 1986 with a grant of $1m by M^2C along with the clean room. The test mask for this endeavor was provided by National Institute of Science and Technology (NIST) and students carry out in-situ testing as well as exhaustive testing in all stages of processing including Oxidation, Lithography, Diffusion, Metallization etc. Phase 4: This phase was not also accomplished because of budgetary and space problems at our place so far.

1. Introduction

"Theory without practice is Utopia and practice without theory is superstition" has been the guiding beacon in imparting the instructions by the author all along. It is because of this reason the VLSI design laboratory was established simultaneously with the development of VLSI Design courses (16.502/16.470). In 1984, only text book available was Mead and Conway and DLAP was the prime tool for the experimental layout and simulation. The projects were fabricated at M^2C, and were tested at UMASS Lowell using LV 500 tester.

Full use was made of both of these in the class room as well as in the laboratory. Since it involved extensive use of programming in PASCAL, along with VAX operating instructions it did slow down the layout, so project such as Flip Flops, LIFO's, FIFO's along with basic gates could be completed. In 1985, Berkeley however, releases MAGIC through M^2C, which was a mouse driven drafting tool. It helped in getting bigger projects consummated during the semester such as ALU's recursive filters, traffic light controllers etc. Advanced books on CMOS design by Neil Weste also appeared which provided an ideal mix of theory and experiment which author followed real rigorously. Course syllabus can be viewed at *http://ece.caeds.eng.uml.edu/*. In 1994, author developed an advanced VHDL based design course (16.602), wherein it became evident that MAGIC is very slow for keeping up with advances in VLSI technology.

It is with this view in mind Cadence/SUN laboratory was established, wherein all four design bundles are available as simulation and synthesis tools. Project such as 16 bit CPU, intelligent traffic controller, Booth multipliers, Priority encoders, BCD encoders, Odometers etc. have been designed, simulated and verified in this laboratory. In the class room, instructions are being imparted, which encompass issues such as gate delays, heat dissipation, noise margins, speed, sub threshold leakage, area estimation, challenges and trade offs on designing chip etc. Advanced graduate projects, M.S. and Ph.D. theses are being produced because of these lab facilities, including a complete transport Protocol chip set designed in this laboratory and fabricated at MOSIS.

The speed enhancement through software has also been the cardinal philosophy while designing the VLSI chip e.g. 4-bit *look ahead carry adder* design was imparted using the following equations instead of ripple carry adder, which halved the gate delays.

$C_{i+1}=P_iC_i'+G_i$

$Si= P_iC_i'+P_i'C_i$

$C_i=A_iB_i$

$P_i=AB'+A'B$

Another example is the use of modified *Booth encoder* which allows higher radix parallel operation without generating 3Y multiple instead of using partial products based on:

$3Y = 4Y-Y$

$2Y = 4Y-2Y$

Phase II has however not been achieved so far because of budgetary constraints.

Phase III is accomplished in its entirety because of DSIPL. Herein not only the theoretical instructions on Oxidation and Diffusion based Deal-Grooves model and Fick's model respectively are imparted but their authenticity verified through experiment e.g.

The thickness' is not only calculated from based on Deal-Groove model

$$d^2 + Ad = B\,(t+\tau)$$

but also measured in DSIPL using ellipsometry . The PN junction depth 'x_j' is not only calculated based on Fick's laws resulting into Gaussian distribution for drive-in but it is also measured using Philtec Sectioner.

$$x_j = \sqrt{[4*D*t \ln (C_s / C_{sub})]}$$

The doping concentrations n or p was calculated and were compared against results derived through measurements of thickness and sheet resistance R_s using Dektak and four probe-resistivity meter, respectively based on simple formulas:

$n = 1/\rho e\mu_n$

$p = 1/\rho e\mu_p$

$R_s = \rho/t$

2. Model for Comprehensive Learning/Teaching

Inspiration in my teaching has manifested from 'only those people, who learn how to connect the new information with the existing software in their intellect become wise, else they remain otherwise'. Having contemplated on this theme for a long time, the author developed a comprehensive model for VLSI education. This was presented at the Canadian Conference on Engineering Education ($C^2 E^2$) at University of Novas Costia in 1998, which received wide acclaim from the academia and industrial leaders, thereafter. The model primarily consists of five phases: 1) Fundamentals 2) Materials 3) Devices 4) Circuits and 5) VLSI system. Each phase has to be taught and learnt by students in their entirety as depicted in Figure 1. A comprehensive testing and verification for learning assessment has been developed for all these phases in order to prepare the students for 21st century.

Most of the fundamentals are learnt through Chemistry, Physics, Mathematics and Digital Logic courses. Heavy emphasis is however laid upon Silicon, which is in the IV group of the Mandleef's table and serves as primary semiconductor element. As an atom it depicts $1s^2 2s^2 2p^6 3s^2 3p^2$ in its orbital configuration. As an element in the material form, it however becomes $1s^2 2s^2 2p^6 3s^1 3p^3$. That means splitting of the outermost energy levels takes place, which is called hybridization as shown in Figure 2. This is the starting juncture of semiconductor theory, which delineates into empty conduction band (CB), full valence band (VB), with an energy gap 'E_g' separating the bands. This forms the basic p-n junction. The p-n junction fabricated back to back forms the Bipolar Junction Transistor. Unipolar transistor such as MOSFET devices are integral parts in making circuits such as inverters, logic gates, and Flip Flops etc. Putting these circuits in a special sequence leads to the formation of VLSI systems. The specifications for such system emerge from the requirement of the customers. In order to comprehend this in their entirety, numerous assignments are required to be completed, along with a detailed project including its design, simulation and verification. These are vital assessment tools employed in the class room and the laboratory.

3. Blending of Engineering Fundamentals with State-of-The-Art Technology

After establishing the laboratories in VLSI Design and Fabrication in 1984 and 1986 respectively, these facilities have been upgraded continually. In addition, pertinent courses for the VLSI Design and Fabrication were developed and taught and the author has been teaching these courses all along. The courses in the area of Computer networking and MMIC technology were also developed. All these courses deploy a proper mix of engineering fundamentals and training at state-of-the-art technologies for preparing the students to withstand the challenge of global competition.

The author felt astonished, how deep this topic was germane to the industry as revealed at the 50th anniversary of American Electronic Association celebrated at the Motorola Campus at Schaumburg Illinois in 1995. Executive V.P. of Motorola articulated in his inaugural address, "Industry neither has the resources nor will to train the people. Universities will have to do both i.e. teaching fundamentals as well as training the students on some state-of-art technology, so that they are productive right away". Dr. John White (Dean of Georgia Tech, then) said, "Our job is to teach Fundamentals". Motorola's executive V.P. said, "You will be history, and to prove my point I am award ing $1 million to Purdue University to come out with an integrated curriculum, which will accomplish both". I came overwhelmed with enthusiasm and shared this conversation with our former Chancellor William T. Hogan who said, "This is our mission in the university". I felt deeply relieved, that we were doing the right thing.

The author involved leaders namely Robert Meisenhelder and Robert O'Reilly from Analog Devices, George LeVan, Drs. Bradley Barber, Stan Swearingen, and Vinay Kulkarni from Skyworks Solutions, Drs. John Vaughan and Greg Henderson from MA/Com, John Beck and Rob Richardson from Intel. The issue of integrated curriculum is of prime importance to these national leaders. Preparing the students at UMASS Lowell with a proper mix of engineering fundamentals and training at state-of-art technology, so that they are productive on the job right away. It is because of this sublime endeavor of the department in general, and that of the author in particular, there is hardly any Hi-Tech industry in the nation, where our alumni are not in significant numbers in leading jobs. The DSIPL has celebrated its 20th Anniversary on November 29th 2007, where the Provost Donald E. Pierson has awarded plaques to these industrial leaders.

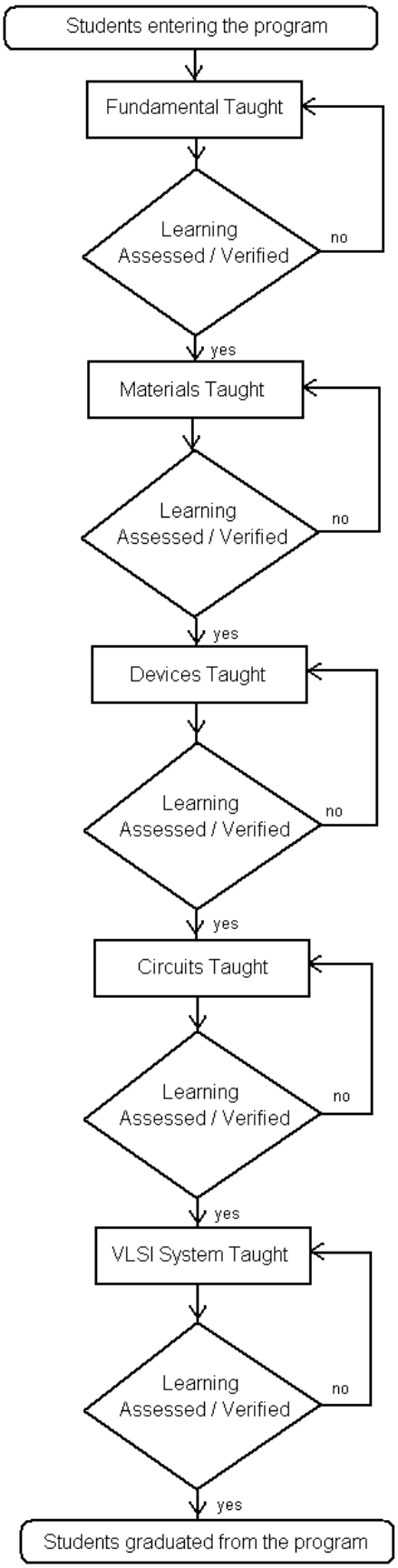

Figure 1: VLSI Education Model

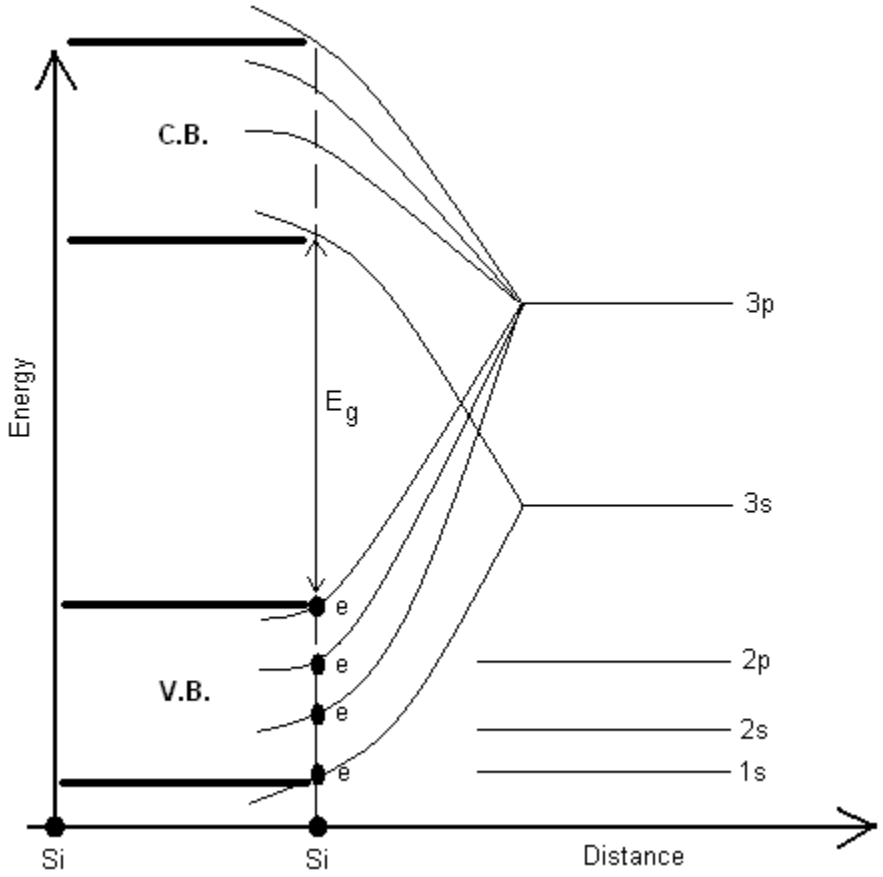

Figure 2: Hybridization Model

4. Conclusion

The system design in general and VLSI system in particular needs multidisciplinary skills. The VLSI education model addresses this problem adequately. In order to become an integral VLSI designer one needs to inculcate skills in design, simulation, testing and verification. This requires a special commitment of funds, which are beyond budgetary allocations of the schools. The partnership between academia and industry is of vital importance which author has envisioned all along, especially through sponsorship of UMass Lowell's VLSI Design and Fabrication activities.

The inception of this program ensued with the grant from M^2C along with a clean room facility. After the demise of M^2C, its support ended. The author approached a number of semiconductor industries in the region such as Analog Devices, Skyworks' Solution (former Alpha Industry), MA/Com, Raytheon, and Intel. These industries have become members and sponsors of this program. The Hi-Tech leaders play a vital role in meeting the growing demand for Microelectronics/VLSI personnel not only in the region, but in the nation as well. It is the contribution and perpetual support of these companies, and the vision of the author, which has kept Microelectronics/VLSI Technology program within the department of Electrical and Computer Engineering at UMass Lowell vibrant.

5. About the Author

Dr. Kanti Prasad is a professor in the department of Electrical and Computer Engineering and is the founding Director of Microelectronics/VLSI Technology program at UMass Lowell. He holds his Ph.D. from University of South Carolina. He is a registered Professional Engineer, P.E., in the State of Commonwealth of Massachusetts. He is the ASEE's campus representative at the James B. Francis College of Engineering. He is also the transfer coordinate and the graduate Semiconductor/VLSI certificate coordinator. He has been teaching and has an industrial experience of 40+ years. He is the author of over 200 theses, dissertations and papers published and presented in journals/conferences of national and international repute.

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