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Presenting Test Benches and Device Characteristics of Programmable Logic In An Introductory Logic Circuits Course

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Abstract

In the fall semester of 2011, we introduced the complex programmable logic device (CPLD) in our introductory logic circuits course. We specifically chose to use a CPLD as it is a modern logic device and includes the use of modern CAD tools and allows for hands-on activities. This paper considers test benches as well as CMOS device characteristics which are each important to the students' learning experience about CPLDs. In our prior research we identified test benches as a critical aspect in the use of logic circuit CAD tools. This paper first outlines our effort to better introduce students to test benches.

Previously, in teaching with traditional TTL logic, the presentation of device characteristics such as signal Voltage levels, device loading, and propagation delay was immediately available. With the move of other educators from such a hands-on, to a hands-off approach using a development board, the presentation of device characteristics appears to be missing from the curriculum. In using our CPLD module we are discovering ways, in the context of CMOS devices, to introduce long standing basic concepts back into our introductory logic circuits course.

Students in such an introductory course must be aware that they are dealing with real circuits and that logic signals are represented with physically measurable quantities. The logic circuits lab must be tangible, demonstrating the connection between digital and analog concepts, such as Voltage and current. Our students take their first electric circuits course the same semester as introductory logic circuits which means that these ideas are new to our students. As such we limit our discussion to presenting the device characteristics of logic circuits.

The device characteristics of CMOS gates differ from traditional TTL devices in several important ways. Students discover that for CMOS the transition region between logic high and logic low is extremely narrow which causes a gate to be sensitive to noise present in a slowly changing input. Given such sensitivity, this paper presents a feedback test circuit useful for investigating the transition region. Also, given that some CPLDs include Schmitt trigger capability, our students investigate how such capability reduces sensitivity to noise. Students also learn about propagation delay and static loading such as that with an LED.

In performing our research we assessed our students' learning experience with our test bench tutorial content, and assessed how device characteristics should be included in our course. We include results and analysis from a student focus group, an anonymous exit survey, and include our own observations.

Introduction

In the Fall 2011 semester when CPLDs were adopted for our introductory logic circuit course we used an integrated approach, including the use of CAD tools and a hands-on experience with a breadboard. Our students first used discrete logic devices in two laboratory experiments and then

a used CPLD module. Based on our research[4] we found that in using this module, students can easily identify the CPLD and with modest wiring they can construct circuits that they feel are both satisfying and engaging.

This paper documents our efforts during the Fall 2014 semester to further integrate the Complex Programmable Logic Device (CPLD) into our introductory logic circuits course. This paper considers how to better present test benches as well as CMOS device characteristics, both of which are important to students' learning experience about CPLDs. In our prior research we identified test benches as a critical aspect in the use of CAD tools. Also we consider device characteristics, which some other courses no long cover, to be an important part in an introduction to logic circuits. For the Fall 2014 semester we started with several clearly defined, achievable goals in furthering the integration of CPLDs in our introductory logic circuits course.

1. Improve and expand the presentation of test benches in our tutorial, adopting more of a just-in-time type format. Based on prior feedback that some students are having significant difficulty with modifying test benches, we made this improvement a priority.

2. Consider pedagogy topics related to test benches and also consider the effectiveness of the tutorial as a reference.

3. Develop new content to better introduce device characteristics. It has always been our concern that our students be aware that they are dealing with real circuits and that logic signals are represented with physically measurable quantities.

4. Upgrade the ISE tools to the latest version, which is 14.7. In our experience versions 13.2 and 14.7 are very similar so we did not expect any change in our student's experience.

Our University offers Bachelor of Science degrees in both Electrical Engineering (BSEE) and Computer Engineering (BSCmpE). The introductory logic circuits course and lab are required for our BSEE and BSCmpE students but is the first in a sequence of courses taken by BSCmpE students. Although the majority of our students are BSEE and BSCmpE majors, there are some from Computer Science, Math, Mechanical Engineering, and others.

Our BSEE and BSCmpE students take logic circuits during the first semester of their sophomore year, the same semester that they take their first course in circuits theory. Our logic circuits course serves as a gateway to the following courses. Courses that are required by BSCmpE and are electives for BSEE students are marked with *, courses that are electives for BSEE as well as BSCmpE are marked with **.

- ECE234 Digital design using CPLD*
- ECE332 Microprocessor applications
- ECE335 Computer architecture*
- ECE336 Computer systems laboratory*
- ECE532 Embedded microprocessor**
- ECE534 VHDL and applications**

The use of test-benches is an important aspect in the use of a logic circuits CAD tool. Without having a graphical tool available for generating a test bench our students modify a skeleton test bench that is generated by the CAD tool. Given that it is not a course goal to teach our students a hardware description language, we took steps to improve our tutorial by adopting more of a just-in-time approach that we outline.

Also, we feel that in such an introductory course students must be aware that they are dealing with real circuits and that logic signals are represented with physically measurable quantities. We feel that it is necessary to demonstrate the connection between digital and analog concepts. First, we have our students measure the threshold for a gate. Given that CPLDs may include Schmitt trigger capability, it is necessary to show how that feature reduces sensitivity to noise. Also, it is important to better examine the cause of propagation delay. Our students use an oscilloscope to measure propagation delay and learn how to select a load resistor for a device such as an LED.

To assess our results we used an exit survey questionnaire and also held a focus group meeting. To help to clarify the feedback from 2014 we present in each section the corresponding relevant data in context, including that from 2012 and 2013. We left out the feedback from 2011 as it is somewhat dated. For the purpose of easy reference we summarize in Appendix A the results for the exit survey in 2014. The Likert value +3 indicates strong agreement, +2 moderate agreement, +1 slight agreement, 0 indifference, -1 slight disagreement, -2 moderate disagreement, and -3 indicating strong disagreement. The list of the labs referred to is in Appendix B.

Literature Review

In reviewing the literature, Radu[12] emphasizes the use of development boards and Coowar[2] elaborates on PLDs as well as CAD tools, but their students did not actually construct logic circuits. Nickels[8] provides a choice between two options, either construct logic circuits using discrete logic devices on a breadboard, or use a PLD on a development board. Nickels rightly points out that the use of a development board eases the development of logic circuits, however with such convenience, Nickels also suggested that electrical and computer engineering students may not have a suitable hands-on laboratory experience. As such, our use of a PLD with a classic breadboard is a very different choice.

With regard to CAD tools Radu et.al.[12] emphasized schematics, but also introduced a Hardware Description Language (HDL) in the context of code fragments and test benches. Wang[13] suggested an integrated approach incorporating breadboard debugging techniques, as well as design and simulation with CAD tools, had students use a development board, and reported positive student feedback. Wang outlines the controversy regarding the use of schematics versus an HDL, expressing a concern that emphasis on an HDL may distract students from the fundamentals of digital logic and suggests that an HDL be taught later, at the junior level.

In our initial planning we followed Wang's advice and chose to not introduce HDLs in our course, but we were later forced to introduce test bench files as the 32-bit version of ISE 10.1 was the last to include a graphical test bench generator tool. In the Fall 2013 semester we upgraded to ISE version 13.2 and discuss later how despite the introduction of test benches, our students prefer the improved stability of the software.

In this paper we consider the usefulness of our tutorial as a reference as well as pedagogy topics related to test benches. In reviewing the literature, Colburn[1], Hawkins[3], and Kolb[7] each outline phases of the learning cycle model and suggest that experiential learning involves reflection to allow for accommodation of new knowledge. We feel that perhaps the lecture and homework can be used as an opportunity for our students to reflect on their experience with test benches in lab.

CPLD Design Procedure

The following outlines how our students use ISE with a CPLD. Students first produce a description of the desired logic circuit, our emphasis is on using schematics like that in Figure 1. The inputs A and B are to the left and the output F is to the right.

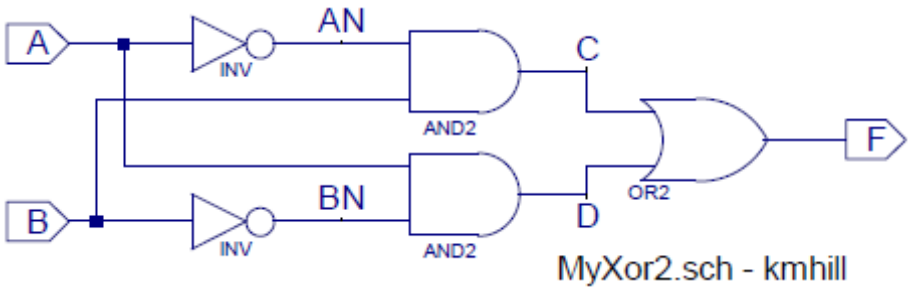


Figure 1: Example circuit schematic

Next, produce a test bench file that describes a sequence of input signals. While a test bench can be made to evaluate the resulting outputs, our emphasis is on visual inspection of the simulation results. In Figure 2 we can see that the circuit behaves like an exclusive-OR gate.

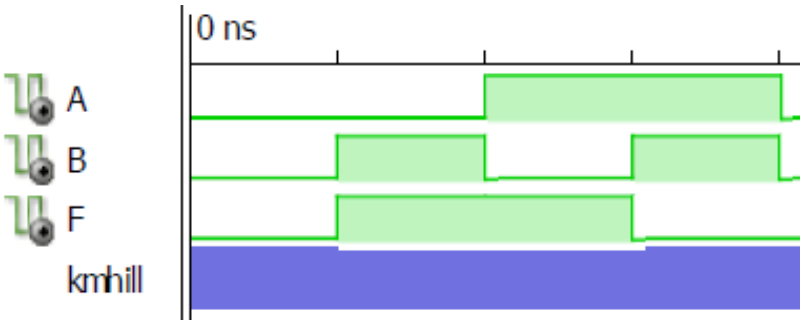


Figure 2: Example circuit simulation

To prepare for the implementation, a constraints file like that in Figure 3 is used to assign the input and output signals to actual device pins. The # character indicates the start of a comment. The signal names are to the left and the pin identifiers are to the right, both in double quotes. A constraints file for a CPLD can be made either with the PACE tool or by typing the text by hand. The ISE synthesis and fitter tools produce the image file which represents the configured logic device and also produce a report detailing how the CPLD resources are assigned. For this example only one CPLD macrocell is used.

```
# MyXor2.ucf - Krista Hill
NET "A" LOC = "P12"; # Mod pin 1
NET "B" LOC = "P13"; # Mod pin 2
NET "F" LOC = "P8";  # MOD pin 40
# end of MyXor2.ucf
```

Figure 3: Example constraints file

Our students next wire a CPLD module into a logic trainer as shown in Figure 4, which provides power (Vcc), ground, as well as inputs (A, B) and the output (F). Once the CPLD is configured using the programming cable, the CPLD will remain configured even after power and the programming cable are removed. Finally, the finished circuit is manually tested.

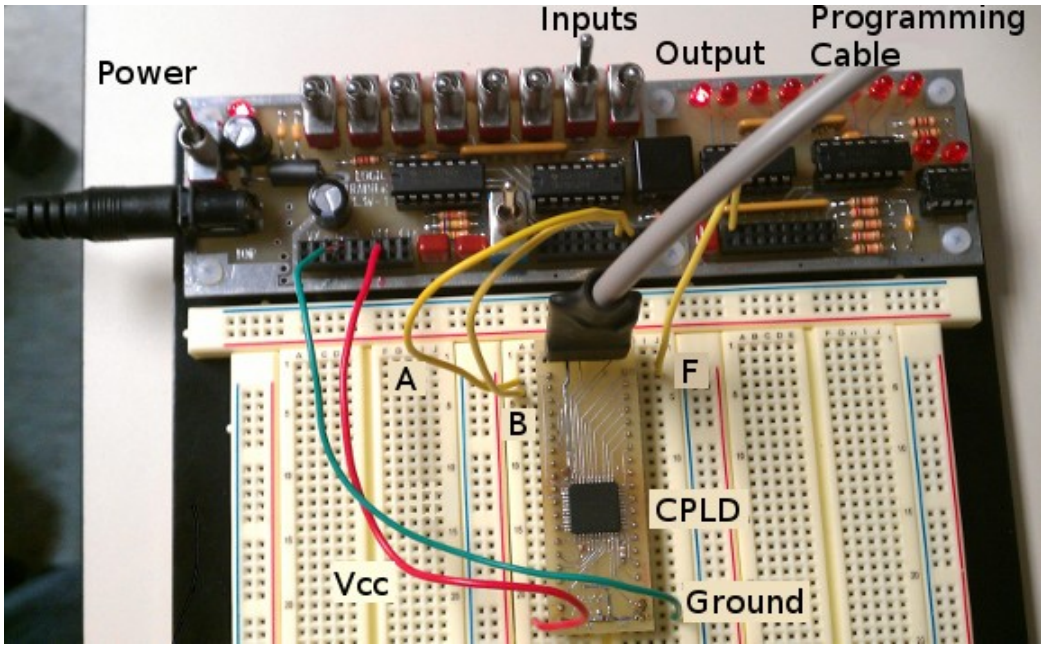


Figure 4: Example circuit being manually tested

In our research the above procedure is not changed. Rather we are improving how we introduce our students to test benches.

Presenting Test Bench Files and Software Upgrade

The tutorial continues to expand as an important element in our use of CPLDs. For the Fall 2014 semester, we updated the tutorial introduction to test benches. We also further upgraded ISE to version 14.7, but without any fanfare. For our tutorial to have more of a *just-in-time* approach, we divided the tutorial into sections and inserted new content as necessary.

- Our students' first use of ISE which considers simple combinatorial logic was expanded with more figures and more code snippets which serve as land-marks in the test bench file. The discussion was also made more descriptive.

- The section on test benches for sequential logic now considers a single flip-flop rather than a state machine. Given that only clock, reset, and input signals are to be generated, a flip-flop provides a minimal context and should help our students feel less overwhelmed.

- New test bench content was added for circuits that make use of multi-bit input and output signals. This content was added to the tutorial hierarchy section where students use a pair of full-adders to make an adder circuit for two-bit values.

Let's consider the ISE software versions. Prior to the Fall 2013 Semester we realized that our students concerns that the 32-bit version of ISE 10.1 was unstable far outweighed the usefulness of its graphical tool that generates test bench files. Subsequent versions of ISE do not include the GUI tool. To ease the burden of making a test bench, ISE generates a skeleton file that our students hand edit to suit their needs. To be able to edit a test bench file we introduce our students to only a measure of VHDL. In reviewing the exit surveys from the Fall 2012, 2013, and 2014 semesters we considered question 22, which in the 2012 data was Q12a and in the 2013 data was Q10

- From 2012 to 2013 the average Likert score improved significantly from 1.28 to 2.29, despite that in 2013 students were hand editing test bench files.
- In the Fall 2012 semester it was the large standard deviation that motivated us to update the ISE software. In the Fall 2013 data the increased average and reduced standard deviation convinced us that upgrading to 13.2 was the correct decision.
- For the 2014 data we consider that fewer responded so that we do not see a significant difference in the average value or standard deviation from the Fall 2013 data.

Question 22		2012(Q12a)	2013(Q10)	2014(Q22)
The CAD software used to draw schematics and configure the CPLD was useful and effective.	Avg	1.28	2.29	2.00
	Std	2.14	0.85	1.00

In 2013 we collected our first data on student use of test benches and consider Q20 which was previously numbered as Q9c. Back in 2013, according to the focus group and the lab instructors, most students found it challenging to modify a skeleton test bench file but a small number of students had particularly significant difficulties. While the average value for Q20 indicated slight to moderate agreement, we were concerned with the standard deviation. After probing the focus group and reviewing the collected feedback we decided that for the Fall 2014 semester it would be a priority to improve the tutorial.

Question 20		2012	2013(Q9c)	2014(Q20)
The online tutorial helped me learn to write the simulation test bench	Avg	– –	1.53	1.9
	Std	– –	1.84	1.6

With the improved tutorial, in the first use of ISE we immediately received compliments from

the lab teaching staff regarding the improved experiences of our students. In reviewing the feedback we can see that the average score for Q20 improved significantly and the standard deviation reduced, suggesting that improving the tutorial was a good choice.

Presenting Test Benches

In this section we consider how having skeleton test bench files and the tutorial impact the student experience. The data from Q24 was unexpected as the student's opinion of skeleton test bench files generated by ISE dropped significantly in 2014, from modest-agreement to slight-agreement, with a slight increase in standard-deviation. We hypothesize that the improved tutorial helps our students to feel more confident in modifying test benches and thus appreciate skeleton test bench files less.

Question 24		2012	2013(Q12)	2014(Q24)
The skeleton test bench generated by the Xilinx test bench generator provides a convenient means for me to produce a test bench, without having learned VHDL language.	Avg	– –	2.06	1.1
	Std	– –	1.43	1.6

We next consider Q9. In 2012 test benches were not yet a topic and students generally agreed that there should be more CAD related topics in lecture. With their introduction in 2013 the interest dropped, and then in 2014 the interest returned. We hypothesize that the improved presentation of test benches in lab helps our students to appreciate such topics.

Question 9		2012(Q4b)	2013(Q4b)	2014(Q9)
There should be more topics related to CAD tools presented in lecture	Avg	2.13	1.47	2.1
	Std	1.13	1.17	1.3

With regard to content we consider Q17. In 2013 with the introduction of the test bench file in lab there was a significant drop to less than slight agreement in having CAD and CPLD topics in homework and then slight agreement in 2014. We see that in 2013 our students felt overwhelmed by the new test bench content and were more at ease in 2014.

Question 17		2012(Q10b)	2013(Q8b)	2014(Q17)
It would be a benefit to incorporate exercises involving CAD tools and CPLD topics into the homework.	Avg	1.60	0.41	1.1
	Std	1.51	1.37	1.1

In reviewing the data we propose that for the next offering that a small amount of lecture content be prepared for the purposes of providing a somewhat global view of the value that HDLs have in industry, and also for reflecting on our student's laboratory experience. Colburn[1], Hawkins[3], and Kolb[7] warn that without reflection, students only parrot content given to them. For VHDL our CPLD course (ECE234) provides our BSCmpE majors with more detail and for a comprehensive treatment our students can take our VHDL course (ECE534) as an elective.

The Tutorial as a Reference

In writing the tutorial our first motivation was for students to quickly start using the CAD tools. The feedback from Q18 suggests that we are successful in that regard. However, given the new just-in-time format, we are curious about our student's experience with the tutorial later in the semester and considered Q21 as well as Q19 which is another reference area.

We are not sure why the Q18 data from 2012 and 2013 is similar or why in 2014 there was a drop in the average from moderate-agreement to between slight and moderate agreement, and a significant increase in the standard deviation. The data for Q21 initially showed an increase but otherwise shows moderate-agreement with some disagreement between students.

Question 18		2012(Q11a)	2013(Q9a)	2014(Q18)
The online tutorial was helpful in getting me started using CPLDs.	Avg	2.00	2.06	1.5
	Std	1.00	0.83	2.1

While the Q21 data is good, in 2014 the scores did not improve. Likewise despite improvements to the tutorial hierarchy section there is a slight decline in Q19 data. In consideration, we have noticed that our students are now asking fewer questions about hierarchy. We hypothesize that with the additional related lab and lecture content, our students now make less use of the tutorial in this regard. We also note that some students were not aware of the sections in the tutorial.

Question 21		2012(Q11c)	2013(Q9d)	2014(Q21)
The online tutorial served as a useful reference to me, later in the course	Avg	1.73	2.00	2.0
	Std	1.85	1.22	1.8

Question 19		2012(Q11b)	2013(Q9b)	2014(Q19)
The online tutorial helped me learn the principle and application of hierarchy.	Avg	2.09	1.76	1.6
	Std	0.83	0.90	1.2

Examining Device Characteristics and Considering Start-Up Sessions

Our BSEE and BSCmpE students take their logic circuits course in the same semester as their first course in circuits theory. To allow our students to first become familiar with circuits theory, in 2014 we presented logic device characteristics in lab 9, later in the semester. Unfortunately we learned later from the questionnaire that 55% of our students indicated that lab 9 was their least favorite. Our student's dissatisfaction is also evident in Q11, Q12, and Q13. Despite the slight agreement with the questions, the standard deviation is large indicating disagreement among students.

	Question	Avg.	Std.
Q11	Measuring the threshold voltage of the 74HC04 inverter in Lab 9 is educationally relevant and is a good use of my time.	0.9	1.5
Q12	Observing the "noise immunity" behavior of Schmitt trigger using the 74HC14 inverter in Lab 9 is educationally relevant and is a good use of my time.	1.1	1.2
Q13	Measuring the propagation delay with different capacitive load in Lab 9 is educationally relevant and is a good use of my time.	0.9	1.3

The above questions stand in contrast with our students experience with discrete logic, for which we consider Q10. Despite the additional content on devices characteristics in 2014, our student's interest in having an early experience with discrete logic improved from 2013 to 2014, which would seem contrary.

Question 10		2012(Q5a)	2013(Q5a)	2014(Q10)
Having some experience with 74HC discrete devices, in the first two labs, is educationally relevant and is a good use of my time.	Avg	2.27	1.29	2.1
	Std	0.90	1.21	1.3

For the standard deviation in Q10 consider Q2 which tells us that 27% of our students in 2014 had prior experience with discrete logic circuits in high school. In probing our students, we found that our approach to device characteristics had issues. First, our BSEE and BSCmpE students felt that lab 9 was out of place and should be presented earlier along with discrete logic devices. Second, other students including those from Computer Science without a background in circuits theory have always felt unprepared in this regard, to some extent.

To level the playing field with respect to basic circuits theory and basic gates (AND, OR, NOT), in our next offering we will make use of a start-up lab session, scheduled before the first official lab is performed. We will provide our students an experiential learning session like that described by Kolb[7] involving cooperative learning and hands-on activities. In being a start-up session our students will produce only a brief writeup.

It is also important to tell our students that CMOS devices are susceptible to static discharge so that in using such devices they should work in an environment that reduces the chance of static discharge. Having lab benches grounded along with conductive mats and wrist straps helps to reduce the risk in handling such devices. In particularly dry areas a humidifier helps as well.

Examining the Transition Region

Let's we look closer at what we mean by *logic-low* and *logic-high*. Useful references include Kang and Leblebici[6] as well as Hodges, Jackson, and Saleh[5]. Figure 5 outlines the NOT gate model that we use. With respect input Vi, the output Vo is *low*, *high*, or in the *transition region*. The power supply is Vcc and the threshold Vth, where Vi and Vo are the same.

In the *transition* region, with respect to Vi the circuit acts like an amplifier. Unfortunately, to investigate the transition region, a divider circuit formed with a potentiometer has little practical

value. It is well known[11] that in the transition region the gate is sensitive to probe noise as well as power supply perturbations. In approaching the transition region only a slight change to the potentiometer causes the output to switch suddenly between logic values.

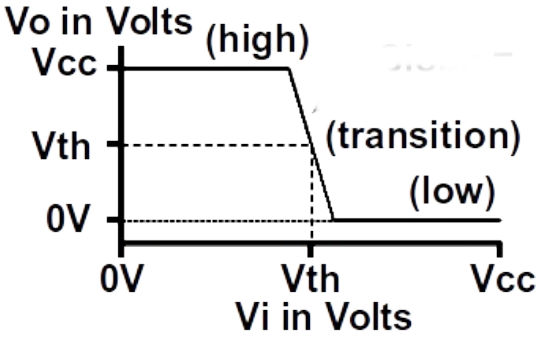


Figure 5: Voltage characteristic for NOT gate

Rather, to measure the threshold Voltage Vth our students used the circuit in Figure 6 to force the gate into the transition region. In using this circuit capacitor C1 prevents oscillation which would otherwise likely happen. To measure Vth, leave the input Vs disconnected and measure the output Voltage Vo. Resistor R2 allows the circuit to be perturbed, to investigate the device behavior. The changes in Vi will only be a few milliVolts so it is important to have the improved precision provided by a lower Voltage scale. With most multimeters the 2Volt scale is adequate.

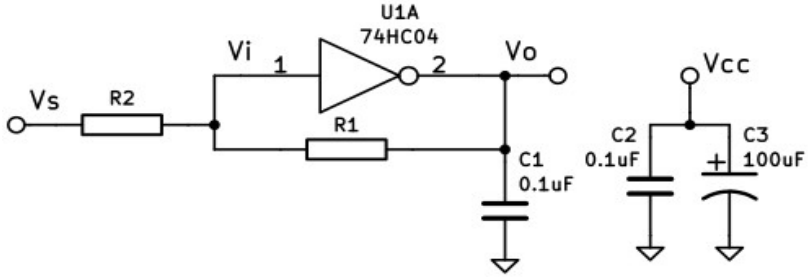


Figure 6: Test circuit for transition region

We have since refined the transition region test circuit to that that shown in Figure 7. The new circuit has the same general simplicity and also allows for direct measurements of Vi and Vo. The circuit uses only the given power supply Vcc and is easier to adjust than the prior circuit. To measure Vth, as before have no connection to Vs. To examine the more positive side of the output transition region connect Vs to ground and adjust the potentiometer. Likewise to examine the more negative side, connect Vs to Vcc and adjust the potentiometer.

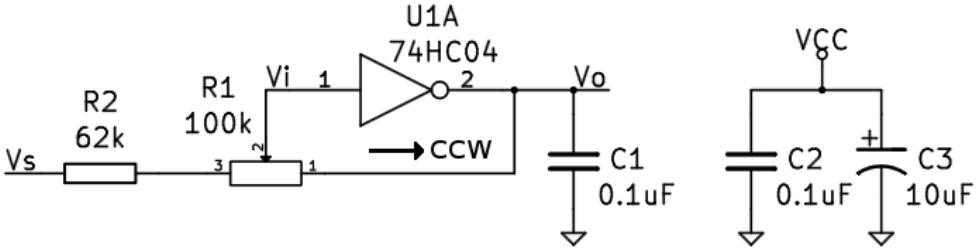


Figure 7: Refined test circuit for transition region

Unfortunately, given that in the transition region the overall gain is large and highly non-linear, it is difficult to characterize such a gate as an amplifier.

Slow Inputs with Noise

With an ordinary CMOS gate erratic behavior is seen when a slowly varying input Voltage containing noise is close to the transition region. To understand such behavior consider that the input transition region for a CMOS gate is very narrow. Figure 8 illustrates the behavior of a NOT gate with such a signal.

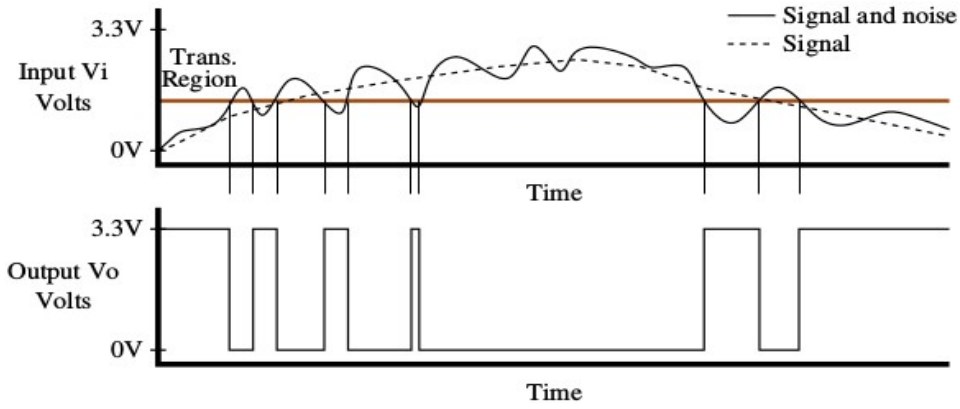


Figure 8: Slow input signal with noise and standard NOT gate

A Schmitt trigger type gate helps to reduce the effect of such noise. Having two threshold values causes the gate to act like a trap. Consider Figure 9 and suppose the output is V_{oH}. Once the input increases to V_{iH}, the output drops to V_{oL} and will remain there until the input is reduced significantly to V_{iL}. When the input is actually reduced to V_{iL}, the output jumps to V_{oH} and will remain there until the input increases significantly back to V_{iH}. The point is that for the gate to change value, the input must change a significant amount. The difference between the thresholds is called the *hysteresis* V_{hys}.

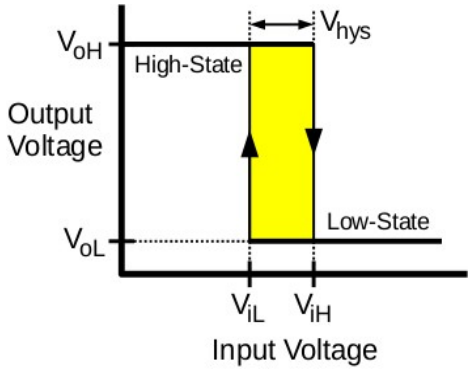


Figure 9: Hysteresis loop for Schmitt NOT gate

In Figure 10 the input has the same waveform as that in Figure 9, but the output is entirely different. This test is performed first with a 74HC04 NOT gate and then with a 74HC14 Schmitt

trigger gate. The 74HC04 gate allows us to examine such a gate without hysteresis.

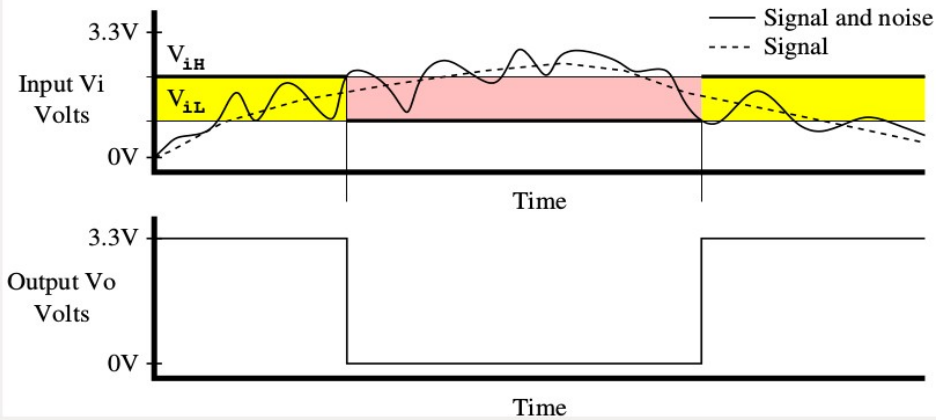


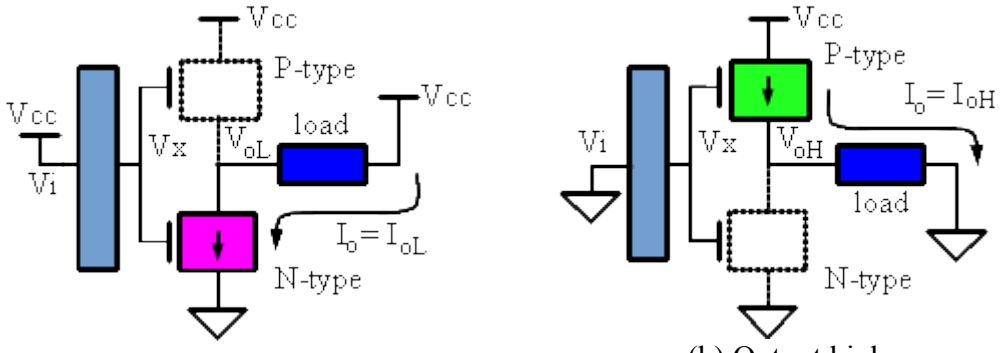
Figure 10: Slow input signal with noise and Schmitt NOT gate

The XC9536XL CPLDs provide a small amount of hysteresis and Coolrunner-II CPLDs provide the option of having hysteresis on a pin by pin basis. In using such gates the benefit of using Schmitt trigger capability should made clear to our students.

Device Loading and Propagation Delay

With CMOS logic the loading and propagation delay behavior is characterized differently than with 74LS logic. We use the term *gate loading* to refer to what happens to an output when current is drawn by a load and the term *drive* to describe the requirements of a given load, and we consider the static and transient cases separately.

Given that our students take circuit theory in the same semester, they are not prepared to discuss electronics. The technology used to make CMOS logic gates is shown below in Figure 11 in a simplified format that emphasizes what the circuit does. In part (a), current into the *N-type* box causes Vo to be *low*. In part (b) current from the *P-type* box causes Vo to be *high*. A single 74HC04 gate uses several inverter stages in cascade, so that the output of one stage connects to the input of the next. The preceding stages are shown to the left in the vertical box.



(a) Output low (b) Output high

Figure 11: Inverter stage

Figure 12 shows the output current-Voltage characteristic. First, when Vo is small the output acts more like a resistor as indicated by the line Gs which intersects with the graph origin. When Vo is larger the output acts more like a current source as indicated by the line Is, which has no slope.

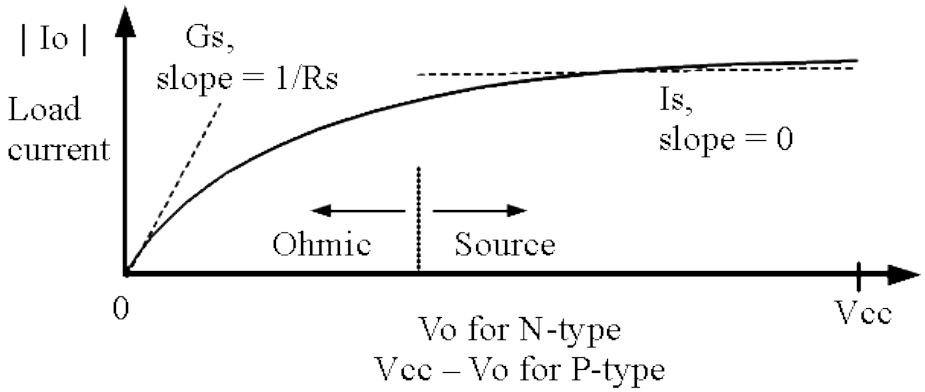


Figure 12: Current-Voltage characteristic

In driving a static load like the LED shown in Figure 13, to reduce the power dissipated in the gate it makes sense to have the gate output more in the Ohmic region. In this case the gate output appears as a resistor Rs in series with R_Y.

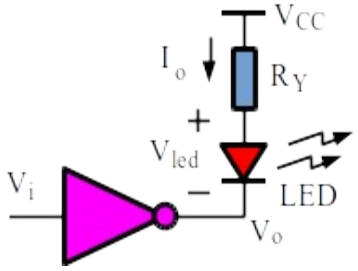


Figure 13: LED drive circuit

In the transient case, the input to a CMOS logic acts like a small capacitor. For a gate to transition between states, the output is initially in the source region and in time changes to the ohmic region. In modeling propagation delay there is an internal delay followed by the time to charge or discharge the attached capacitive load, respectively to Vm, as shown in Figure 14. The manufacturer defines Vm to be one half of the power supply Voltage.

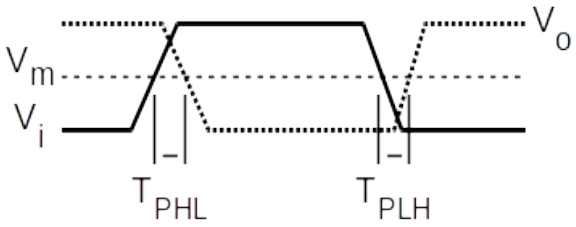


Figure 14: Measuring propagation delay

In considering propagation delay, having the gate output primarily in the source region makes the math simple. The Voltage across a capacitor is proportional to charge and given a constant current the charge is proportional to time. Measuring propagation delay is complicated by the

probe itself which acts like a capacitor. Be sure to use a X10 probe which has less capacitance than a X1 probe. As shown in Figure 15, our students use an oscilloscope to measure delay with several load capacitor values roughly the same order as 50pF, which is the manufacturer specified value.

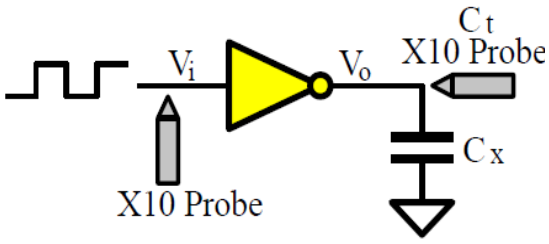


Figure 15: Propagation delay test circuit

In graphing the low to high and high to low propagation delay versus capacitance we expect straight lines. If the oscilloscope and probes are limiting in bandwidth then some measurements will not appear on the lines.

Conclusions and Future Work

The improved tutorial content regarding test benches was well received, though not all of our students were aware of all the new content. For our next offering we will have a small amount of lecture content to provide a more global view of the value that HDLs have in industry, and also to have our students reflect on our their laboratory experience. Colburn[1], Hawkins[3], and Kolb[7] warn that without reflection, students only parrot content given to them. Our CPLD course (ECE234) provides our BSCmpE majors with more detail and for a comprehensive treatment our students can take our VHDL (ECE534) course as an elective.

With regard to presenting content related to device characteristics, our students overwhelming feel that the content should be should presented much earlier in the semester, when they use discrete logic devices to build their first logic circuits. With regards to circuit theory and basic gates (AND, OR, NOT), to level the playing field, before the first lab we will provide our students with a brief summary list of necessary topics and in a manner similar to Kolb[7] we will give our students an experiential learning exercise involving cooperative learning.

References:

1 A. Colburn, "*An Inquiry Primer*," Science Scope, march 2000
2 R. Coowar, "*The Development of a Course in Programmable Digital Devices*," ASEE National Convention, 1996, session 2648
3 D. Hawkins, "*Messing About in Science (1965)*," The Informed Vision, Essays on Learning and Human Nature, Agathon Press, 1974
4 J. Hill, Y. Yu, "*The CPLD Provides a Third Option in the Introductory Logic Circuits Course*," ASEE National Convention, 2012, session W516, AC 2012-5302
5 D. Hodges, H. Jackson, and R. Saleh, Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology, third edition, copyright 2004 by McGraw-Hill.
6 S. Kang and Y. Leblebici, CMOS Digital Integrated Circuits, third edition, copyright 2003 by McGraw-Hill.
7 D. Kolb, "*Chapter Two: The Process of Experiential Learning*," Experiential Learning, Experience as The Source of Learning and Development, copyright 1984 by Prentice-Hall.

8 K. Nickels, "*Pros and Cons of replacing discrete logic with programmable logic in introductory digital logic courses,*" ASEE National Convention, 2000, session 2532
9 NXP Semiconductor, "74HC04; 74HCT04 Hex inverter Product Data Sheet," 74HC_HCT04, Rev. 4 – 3 August 2012.
10 NXP Semiconductor, "74HC14; 74HCT14 Hex Inverting Schmitt trigger Product Data Sheet," 74HC_HCT14, Rev. 6 – 19 September 2012.
11 Philips Semiconductors, "Data Sheet, Family Specifications, HCMOS Family Characteristics," Integrated Circuits, IC06, March 1988
12 M. Radu, C. Cole, M. Dabacan, and S. Sexton, "Extensive Use of Advanced FPGA technology in Digital Design Education," ASEE National Convention, 2008, session 2139
13 G. Wang, "Teaching Digital Logic Using CAD Tools in a Teaching-Oriented University," ASEE Annual conference, 2005

Appendix A

The following are the results for the exit questionnaire. In earlier sections we outline all our feedback in context, along with additional data from our two prior years. Our questionnaire had four categories of questions:

Questions 1 through 4 were intended to be used to form categories of students. We wanted to know (1) which of two lab instructor each student had, (2) whether each student had prior experience with logic circuits in high school, (3) what type of personal computer each student had, and whether or not the ISE software was installed

QN	Question	Data
Q1	Who is your lab instructor?	3: Iman 8: Dom
Q2	Do you have prior experience with TTL or CMOS discrete digital logic devices in high school?	3: Yes 8: No
Q3	What type of personal computer(s) do you have?	8: windows 2: mac 1: Uni. PC
Q4	Regarding installing Xilinx ISE Webpack 14.7 on your own computer? • 1: I successfully installed it on my own computer. • 1: I tried but did not succeed. • 6: I thought about installing it but never actually tried to. • 1: I would have tried if my computer is compatible. • 2: I do not want to install it on my own computer.	

Questions 5 through 24 had Likert scores where +3 is strong agreement, +2 moderate agreement, +1 slight agreement, 0 indifference, -1 slight disagreement, -2 moderate disagreement, and -3 indicating strong disagreement. In the following table the right-most columns provide the mean or average as well as the standard deviation.

QN	Question	Avg
Q5	Using CPLDs in the Logic Circuits course is an overall improvement.	2.3
Q6	The lab projects using CPLDs were interesting and educationally valuable.	2.0

QN	Question	Avg	StD
Q7	My experience with CPLDs makes me more confident and I foresee that in the future I will be more competent as an engineer.	1.7	1.7
Q8	My experience with the CAD tools in logic circuits lab makes me more confident so that in the future I will be more competent as an engineer.	1.7	1.2
Q9	There should be more topics related to CAD software tools presented in lecture.	2.1	1.3
Q10	Having some experience with 74HC discrete devices, in the first two labs, is educationally relevant and is a good use of my time.	2.1	1.3
Q11	Measuring the threshold voltage of the 74HC04 inverter in Lab 9 is educationally relevant and is a good use of my time.	0.9	1.5
Q12	Observing the "noise immunity" behavior of Schmitt trigger using the 74HC14 inverter in Lab 9 is educationally relevant and is a good use of my time.	1.1	1.2
Q13	Measuring the propagation delay with different capacitive load in Lab 9 is educationally relevant and is a good use of my time.	0.9	1.3
Q14	I feel that a laboratory experience in which I construct circuits and investigate signals helps me to better learn the material.	1.5	1.3
Q15	I found that in our use of CPLD in the laboratory, the hands-on experience was retained, and helped me to better learn the material.	1.5	1.4
Q16	There should be more use of CPLD hardware topics in the lecture portion of the course.	1.0	1.7
Q17	It would be a benefit to incorporate exercises involving CAD tools and CPLD topics into the homework.	1.1	1.1
Q18	The online tutorial was helpful in getting me started using CPLDs.	1.5	2.1
Q19	The online tutorial helped me learn the principle and application of hierarchy.	1.6	1.2
Q20	The online tutorial helped me learn to write the simulation test bench.	1.9	1.6
Q21	The online tutorial served as a useful reference to me, later in the course.	2.0	1.8
Q22	The CAD software used to draw schematics and configure the CPLD was useful and effective.	2.0	1.0
Q23	The CAD software helped me make use of and understand hierarchy principles.	1.8	0.9
Q24	The skeleton test bench generated by the Xilinx test bench generator provides a convenient means for me to produce a test bench, without having learned VHDL language.	1.1	1.6

Questions 25 and 26 asked our students for estimates of the longest and average times to generate a test bench. Question 25 asked students to estimate the longest time that it took them to generate the test bench codes for any lab. Among the 11 students who responded: three students chose "more than 40 minutes"; three students chose "20-30 minutes"; four students chose "20-30 minutes"; one student chose "less than 20 minutes".

QN	Question	Data
Q25	Estimate the longest time it took you to generate the test bench codes.	3: More than 40 minutes 3: 30-40 minutes 4: 20-30 minutes 1: less than 20 minutes
Q26	How long did it take you to generate the test bench codes on average?	2: More than 40 minutes 1: 30-40 minutes 6: 20-30 minutes 2: less than 20 minutes

By comparison, question 26 asked students to estimate the average time that it took them to generate the test bench. Among the 11 students who responded: two students chose “more than 40 minutes”; one students chose “20-30 minutes”; six students chose “20-30 minutes”; two students chose “less than 20 minutes”.

Questions 27 through 32 were open ended questions. A summary of student answers is below the table. The list of the labs referred to is in Appendix B.

QN	Question
Q27	What is your largest concern in improving the course? Please elaborate.
Q28	Suggest a laboratory activity involving CPLDs that helps retain the hands-on experience.
Q29	What was your favorite laboratory? Please explain why?
Q30	Which lab(s) were you not able to complete successfully? Please explain why.
Q31	What was your least favorite laboratory? Please explain why.
Q32	Do you have any other comments?

Question 27 asked students what were their largest concern in improving the course. one student expressed frustration with the Xilinx ISE software. One student expressed concern that the lab instructor assumed that all students were in circuits lab and didn’t explain some material. Two students expressed concern in learning to use Xilinx ISE software from scratch following the tutorial in lab with no lecture instruction, one of which also expressed concern that the tutorial was not helpful for programming the test bench in terms of sequential logic and the CPLD sometimes didn’t work properly. Three students had no concern or expressed positive feedback.

Question 28 asked students to suggest a lab activity involving CPLDs that helps retain the hands-on experience. Two student suggested more labs like lab 8 or lab 10.

Question 29 asked students what was their favorite lab. Six students listed either lab 8 elevator controller, or lab 10 digital dice, or both. The reasons that the students listed were mainly because these labs related to real life applications and were demonstrative after completion. One wrote: “When doing these lab (sic), I can see how the things I learned can be applied to real life and it’s cool to see the circuit working”. One wrote: “Lab 10 was my favorite because it helped me understand hierarchical design a bit better, and it was interesting to see it working.” One

wrote: “Lab 8 because I literally got to see exactly what the whole next state meant as regards (sic) flip-flops and what not and it also felt like I could see a practical example of exactly how elevators work on a small scale.” Another wrote: “I liked the dice lab, because it was fun to make an electronic die!” One student listed lab 6. One student listed lab 5 and wrote: “it was well explained in class and was finished with ease”. One student listed lab 3. One student listed lab 2 and wrote: “because it was fun to see how different combinations affect the outputs, and because the lab was new and easy to understand at that time”.

Question 30 asked students which lab(s) they were not able to complete successfully. Among the nine students who provided answers, three students stated that they were able to complete all the labs. Two students didn’t complete lab 10 due to an absence of the lab instructor. Two students didn’t complete lab 8 and 10 due to issues encountered during simulation or pin assignment stage. Three students stated they didn’t successfully complete lab 9. One cited time as the issue, and another cited lack of circuit knowledge as the reason.

Question 31 asked students which lab(s) were their least favorite. Six students cited lab 9 “device characteristics” due to either lack of circuit knowledge or interest. One student stated: “it felt as if it was a more circuits based lab since the logic used within the circuit was limited. This lab was the least interesting due to the lack of logic used in the circuit.” Two students cited lab 8 or lab 10. One student cited lab 1 or lab 2. One student stated: “The next lab usually have something to do with the previous ones, I feel that all the labs are necessary.”

Question 32 asked students to provide any additional comments. Of the four students who provided answers, two students expressed appreciation and general positive feedback toward using CPLD or the course. One student expressed desire for more instruction on how to modify a test bench before each lab. One student expressed desire for more hands-on instruction with Xilinx software.

Appendix B List of Laboratory Exercises from Fall 2014

Lab 1: Digital Gates (Discrete logic)
Lab 2: Verifying DeMorgan's Law and Distributive law (Discrete logic)
Lab 3: Xilinx ISE 14.7 Tutorial Practice
Lab 4: Combinational Circuit Design using Xilinx
Lab 5: Combinational Circuit Design with don't-care conditions using Xilinx
Lab 6: 4-bit Adder/Subtractor and Hierarchical Design
Lab 7: Gray Code Counter using Hierarchical Design
Lab 8: Elevator Controller Design
Lab 9: Device Characteristics
Lab 10: Roll the Dice using 3-bit counter and Multi-level Hierarchical Design