Problem Based Education using a B.A.R.D (beyond a reasonable doubt) Method of Device Characterization of Field Effect Devices

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Abstract

Among the newly developed power IGFETs (Insulated Gate Field Effect Transistors) and systems devoted to automotive electronics in general and microelectronics in particular, some of the prominent characteristics of MOSFETs require studies of high and low W/L ratio geometries and fast polygated devices. The W/L ratio is a measure of the device area as it gives the ratio of channel width to channel length. This paper will discuss parametric issues related to radiation effects, impurity diffusion effects and hostile environments such as the outerspace or nuclear weapon explosions. This paper shows fitting of a linear regression curve, determine its intercepts, slopes and reciprocal of slopes to identify the correct mathematical values of threshold voltage and transconductance of the device under test. These parameters can be used to interpret subthreshold behavior and interface states, reverse short channel behavior and study diffusion of impurities if a hybrid PZT (Lead Zirconate Titanate- 52/48) sensor is located in the vicinity. The program is used to plot and fit the experimental data given out by a HP4145B parametric analyzer. The parametric (I-V) measurements were obtained on a range of devices. These devices are numbered. The number 50 and 52 devices are 50-micron device with 50 micron channel length and 1000-micron channel width (W/L:1000:50) poly silicon gates. The other poly silicon gate devices are all of smaller width of 11.5 microns, and consist of 1.5-10 micron channel length devices. We will analyze and compare the simulation with the experimental values.

Keywords: Enhancing the process of Engineering Education, Problem based Education, Student Research Experience

Introduction

It is important to enhance the understanding of the design and limitations of field effect transistors to undergraduate students. MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistors) are currently the cornerstones of all modern microelectronic circuits. With the new applications of communication satellites and their transits near the radiation off the Van Allen belts, there has been an intensive study into the deteriorating effects of ionization radiation on MOS structures. Furthermore, ever increasing demand of miniaturization of these devices and their processing with energetic photons or particles in the ULSI age, it is very important to study their parametric behavior from both practical and scientific points of view. As semiconductor industry progresses to bigger size wafers 300mm dia. and from VLSI ($2^{16} - 2^{21}$ devices/chip) to...
ULSI ($2^{21} - 2^{25}$ devices/chip), it is possible to technologically hybridize sensors along with circuits.

Diffusion of impurities initiated by normal processing conditions become a major concern when such a process is used in the manufacture of the integrated circuit. Once again I-V or parametric studies of such ICs (Integrated Circuits) involving IGFETs are becoming a concern.

**Uncertainties in I-V Characteristics**

The MOSFET is a four terminal device and its terminals are designated as the source (S), the gate (G), and the drain (D). The substrate or body called as (B) or (SB) forms the fourth terminal as shown in Fig. 1.

![Figure 1. 3-D Cutaway View of an IGFET](image)

The MOSFET is constructed with a metal (Al) gate terminal usually insulated from the channel portion of the semiconductor under the gate connecting the source and the drain with a silicon dioxide dielectric called gate oxide. The IGFETs have a seminsulating silicon gate electrode instead of the metal. It proves to be advantageous to have silicon gate, as it has a broader control on its voltage to turn on called threshold voltage, from materials processing point of view.\(^1,2,3\)

Depending on the type of charge carriers flowing in the channel, an IGFET can be classified as either an n-channel (electron conduction) or a p-channel (hole conduction) device. If the transistor is normally “off” (no current flowing at $V_G = 0$), it is called an enhancement mode device, if the transistor is normally “on” it is called a depletion mode device. In table 1 one can see how the output characteristics of four possible types of IGFETs will look (see Table 1).
X-ray lithography cannot always be avoided in ULSI technology. High temperature anneals and MOS technologies are particularly sensitive to the cumulative effect of ionizing radiation (total dose absorbed in the oxide layer). Therefore, the sub-threshold swing for various short channel lengths are different and increase with V=0.3Vp, the pinch off voltage. In the ideal IGFET, for a uniformly doped channel, the sub-threshold I_D versus V_G is almost a straight line for a long channel device. However, one can see that sub-threshold characteristics for various short channel lengths are different and increase with doping and drain voltage. Therefore, the sub-threshold swing also increases, and threshold voltage typically depends upon the nature of the obtained I-V curves (see Fig. 2).

Radiation Effects

MOS technologies are particularly sensitive to the cumulative effect of ionizing radiation (total dose absorbed in the oxide layer). Process induced radiation, such as E-Beam evaporation, RIE or reactive ion etching, or plasma etching and plasma enhanced deposition processes along with X-ray lithography cannot always be avoided in ULSI technology. High temperature anneals...
cannot be effectively employed. The primary effect of radiation is ionization in the bulk and near the interface of silicon dioxide and build up of charge\(^1\) (see Fig. 3a and 3b).

![Defect Structures](image)

Figure 3a and 3b. Defect Structures

At relatively low doses (10\(^5\) rad (Si)) and for moderate gate oxide thickness (40-100nm) the threshold voltage shift due to charge trapping (holes) can be expressed as \(\Delta V_T = K t_{ox} D\), where \(K\) is proportional to hole trapping efficiency, \(t_{ox}\) is the gate insulator thickness and \(D\) is the total dose. At higher doses, interface traps can build up significantly near the Si-SiO\(_2\) interface and the threshold shift can be written where \(\Delta V_T = \Delta V_{ot} + \Delta V_{it}\), where \(\Delta V_{ot}\) is the contribution of oxide trapped charge and \(\Delta V_{it}\) is the interface contribution.

We can estimate the defect concentration \(N_D\) for corresponding traps, using the equation \(\Delta V_T = \text{Threshold Voltage Shift} = e N_D t_{ox}/\varepsilon_{ox}\), where \(e\) is the electronic charge in Coulombs, \(N_D\) is the aerial defect concentration per unit area, assuming the centroid to be at the interface, and \(\varepsilon_{ox}\) equals the permittivity of the oxide \(\approx 0.34\) pF/cm, as such phenomena and their involvement with the transconductance of the devices raise large uncertainties in interpretation of their threshold voltage etc.

**Hybridized Circuits**

When hybridized circuit components play their role, the process-induced diffusion of impurities such as H\(_2\)O and Pb from a PZT (Lead Zirconate Titanate- 52/48) sensor will (see Fig. 3c) contribute in the annihilation of interface\(^3\) states during the post metal annealing or a similar process.

![Defect Annihilation by H or Pb.](image)

Figure 3c. Defect Annihilation by H or Pb.

Thus, high interfacial-trap concentrations would be severely stunted due to development of such an insulator-semiconductor systems.
The majority of small-perimeter effects in IGFETs are associated with the reduction in channel length $L$. It is, thus, appropriate to define a specific minimum channel length $L_{\text{min}}$, below which short-channel effects (decrease in $V_T$ with channel length, see Fig. 4a) are expected to occur,

$$L_{\text{min}} = 0.4 \times (r_j t_{\text{ox}} (W_S + W_D)^2)^{1/3},$$

where $t_{\text{ox}}$ is the oxide thickness in angstrom, $r_j$ is the source/drain junction depth in $\mu$m, $W_S$ is the depletion width at the source junction, and $W_D$ is the depletion width at the drain junction in $\mu$m. The nature of short channel effect is changed from short to reverse short channel effect, if there is a capping oxide on the top of these short channel devices, as it collects fixed charges. This again (see Fig. 4b) gives threshold voltage variation beyond the regular expected value.

$$V_{\text{DS}} = 0.1V, \quad V_{\text{DS}} = 5V$$

Fig.4a. $V_{\text{DS}}$ Effect on short-channel effect.

Figure 4b. Nature of Short Channel and Reverse Short Channel Effect

The regular value of $I_D$ vs. $V_G$ curve can be given as, $I_D = \left(\frac{W \mu_{\text{eff}} C_{\text{ox}}}{L}\right) \left(\frac{V_{\text{GS}} - V_T}{2}\right)$ shown as (Fig. 5).

$$I_D \text{ vs. } V_{\text{GS}}$$

Figure 5. $I_D$ versus $V_{\text{GS}}$ – Ideal Curve

We have not estimated this in any of the equation but accepted experimental value.

**Experimental Setup**

A Schematic setup of the system for the I-V measurement is shown in Figure 6.
Before one receives the correct data from the measurements, the Semiconductor Parameter Analyzer must be set to proper channel inversion and voltage bias. The probes are connected to the corresponding source, drain, and gate terminals of an IGFET on the processed wafer, and provide the contact for the I-V stimulus through a personality module. P-type wafer with substrate resistivity of 0.1 Ohm-cm was used to fabricate n-type enhancement mode IGFETs. Then (I – V) measurement technique was used by varying the gate from 0V to ~10V on various IGFETs to obtain threshold voltages near flatband conditions. This threshold voltage was the X-intercept of the maximum slope line drawn on the I-V curve. We felt that a better and surer method will be to fit the data using a linear regression method using a straight line from pre-threshold current values up to post-threshold voltages and get a mathematically correct fit.

**Using Kaleidagraph**

When determining the slope or the threshold voltage of the I-V data, we used the Kaleidagraph program, using data from the HP4145B analyzer. The experimental plot was estimated from SigmaPlot using data. The graphs were done in two forms: the original slopes determined by the HP4145B machine and the slope best fitted for Kaleidagraph using a linear regression approximation. The purpose is to determine the X-intercept; m1 is the Y-intercept; and m2 is the slope of the graph. The X-value was the voltage; the Y-value was microamps. Each number on the Y-intercept was determined by the following formula:

\[(\text{Number of small divisions}) \times (\text{8 \times microamps per division})/\text{sum of small divisions}\]

![Figure 7. Original Maximum Slope](image)

![Figure 8. Best Slope Fit by Kaleidagraph](image)
For the original maximum slope (Fig. 7), the slope was 2.01E-06; the Y-intercept was –3.91E-06; and the X-intercept was 1.38. For the best slope fitted for Kaleidagraph (Fig. 8), the slope was 1.82; the Y-intercept was –1.7175; and the X-intercept that was determined was .943681.

Conclusion

We found that it is an accurate working method to find threshold voltage and should have a high correlation with the observed values. This paper provides the knowledge of a creative approach to seniors and beginning graduate students.

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Bibliography


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