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PSPICE Implementation of an 8-bit Low Power Energy Recovery Full Adder

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***Abstract* —Energy recovery technique has attracted interest of low power VLSI designers in recent years. This low power design technique has been proposed and discussed by many researchers. In this paper, we implemented energy recovery technique in the PSPICE using an 8-bit full adder circuit as an example. Full adder circuit has been widely used in arithmetic operations for addition, multipliers and Arithmetic Logic Unit (ALU). It is a building block used in digital signal processing, image processing and microprocessor. An 8-bit low power and low transistor count static energy recovery full adder (SERF) is implemented in this paper. The power consumption and general characteristics of the SERF adder are then compared with the 8-bit traditional CMOS full adder. PSPICE power simulation is used to verify its power consumption for the given input pattern sequence. Simulation result demonstrates effective power saving of the energy recovery full adder compared to static CMOS full adder.**

Keywords —Low Power VLSI, Energy Recovery, Full Adder, PSPICE, Power Simulation.

I. INTRODUCTION

The explosive development in laptop and portable systems and in cellular networks has intensified the research efforts in low power electronics. For portable information systems, power dissipation has a direct bearing on size, weight, cost, and battery life. So power dissipation is becoming widely recognized as a top-priority issue for VLSI circuit design. Nowadays low-power VLSI design has become a major design consideration. Various low power VLSI techniques have been reported [1-2]. Among them, energy recovery technique [3-4] has been a novel and attractive solution. Energy recovery includes any technique or method of minimizing the input of energy to an overall system by exchange of energy from one sub-system of the overall system with another. Energy recovery logic utilizes a different way from standard CMOS logic to charge and discharge node capacitance and can achieve ultra-low power consumption. During the slow charge and recovery process of node capacitance, the power clock together with the clock generator circuit forms a resonant network. The whole circuit dissipation is caused by the path resistance (which is called adiabatic loss) and the voltage difference of the two path ends (which is called non-adiabatic loss) [3]. Based on the power consumption, energy recovery circuit can be divided into fully adiabatic and partially adiabatic circuit. Fully adiabatic circuit can avoid non-adiabatic loss by retractile power clock or reversible logic, both of which are impractical for realization. Partially adiabatic circuit has simpler structure and power clock scheme while consuming much less power compared with traditional CMOS digital circuit, so it is a viable option for real low power applications [4-5]. In [6], design of energy recovery circuits using both reversible and partially reversible logic have been reported.

In [7], implementation of low-power adiabatic computing circuit with NMOS energy recovery logic is reported. In [8], the implementation of complementary pass-transistor energy recovery logic for low power has been proposed. In [9-10], design and testing of energy recovery circuit ad its improvement are proposed. In [11-14], energy recovery D flip-flop and single-phase energy-recovering logic for low-power VLSI design have been reported. Adder is one of the most important building block of microprocessors. High performance and low power Adder deign is critical to the performance of overall microprocessors. Various energy-recovery full adder designs have been reported [15-18]. In [15], a 16-bit carry-lookahead adder using reversible energy recovery logic for ultra-low-energy systems is reported. In [16], quasi-static energy recovery logic (QSERL) uses two complementary sinusoidal supply clocks and possesses several positive characteristics of static CMOS logic. The lower switching activity reduces energy dissipation. In [17], the design of low-power energy recovery adders based on pass transistor logic is discussed. The 14-transistor full-adder [18], as the name implies, uses 14 transistors to realize the adder function. To date this is the most area efficient design. The 14T full adder cell, like the transmission function full adder cell, implements the complementary pass-transistor logic to drive the load. A novel static energy recovery full (SERF) adder (10-transistor design) with reduced power consumption at the cost of increased delay is reported in [19]. The proposed 10-transistor design utilizes low power energy-recovering

technique to reduce the power consumption. It consumes less energy and has a lower transistor count compared to other proposed full adder cells. We use the 10-transisor SERF adder design from [19] in our 8-bit low power energy-recovery full adder design.

II. CMOS FULL-ADDER DESIGN

In order to compare the power consumption with the 8-bit energy recovery SERF full adder, an 8-bit static CMOS full-adder is also designed. The schematic design of 1-bit static CMOS full adder cell [20] is shown in Fig. 1. It consists of two complex gates connected in series: one implements carry-out (Co) and the other implements Sum (S). The carry-out is used to generate Sum. In this project, we use Cadence OrCAD PSPICE to build the circuit. The PSPICE schematic design of the one-bit CMOS full adder is shown in Figure 2.

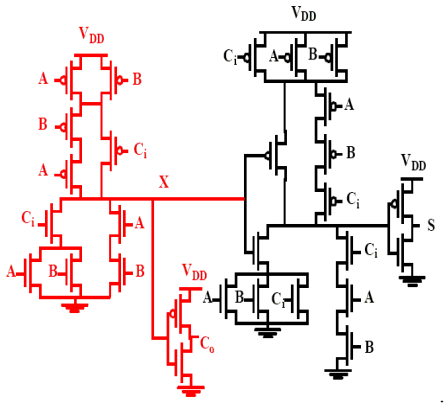

Fig. 1. Schematic of a CMOS full adder [20]

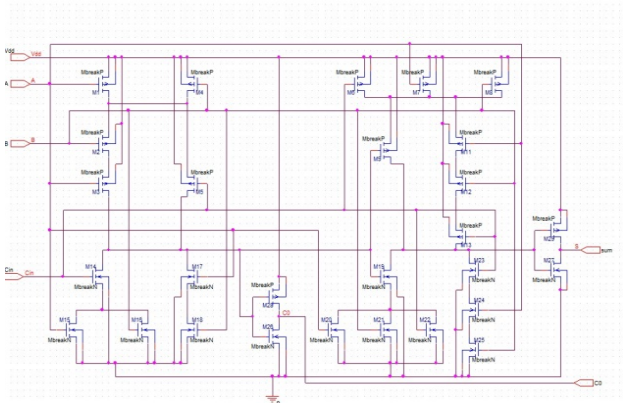

Fig. 2. PSPICE schematic design of 1-bit CMOS full adder

The 1-bit static CMOS full adder contains 28 transistors. The 1-bit CMOS full adder is designed in PSPICE. Its function is verified with PSPICE simulation using exhaustive testing with all the eight test patterns (ABC_i=000~111). After that, it is defined as a block and PSPICE hierarchy design is used to design the complete 8-bit full adder. The 8-bit static CMOS full adder by using hierarchy design is shown in Fig. 3 below.

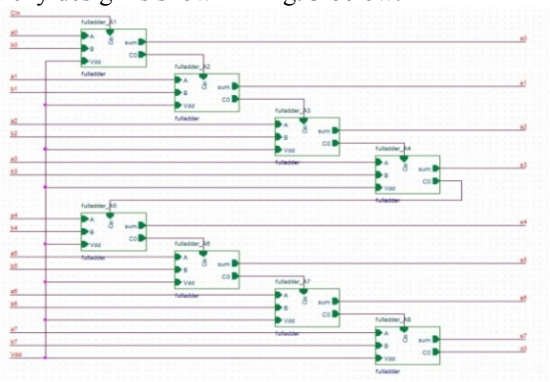

Fig. 3. Schematic view of 8-bit static CMOS full adder

There are 28 transistors in each block, so there are totally 224 transistors in the 8-bit CMOS full adder. In the simulation, I give 8 patterns to both input A and input B.

The input A: $a_0a_1a_2a_3a_4a_5a_6a_7$ = '01111000', '01101010', '11101100', '10001111', '00100111', '00110100', 10110010', '01001010'.

The input B: $b_0b_1b_2b_3b_4b_5b_6b_7$ ='11101010', '11001001', '11010110', '01100111', '00001101', '10111001', '10010001', '11000111'.

The simulation waveforms of inputs (A and B) are shown in Figures 4-5 respectively.

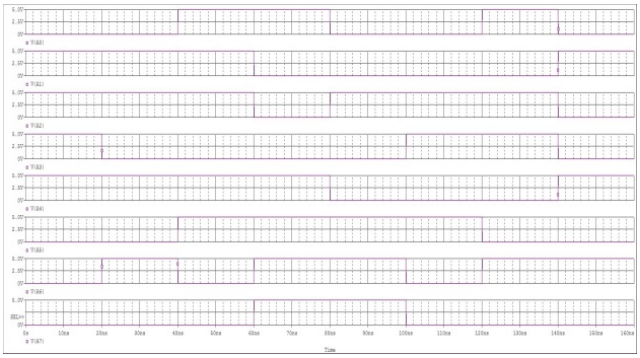

Fig. 4. PSPICE waveforms of input A

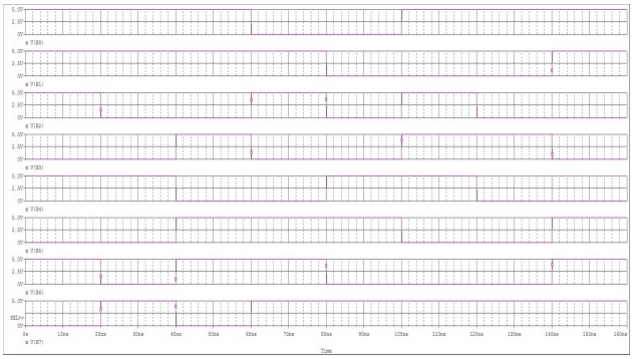

Fig. 5. PSPICE wave form of input B

After using PSPICE simulation, the output waveform of SUM of the designed 8-bit static CMOS full adder is shown in Figure 6.

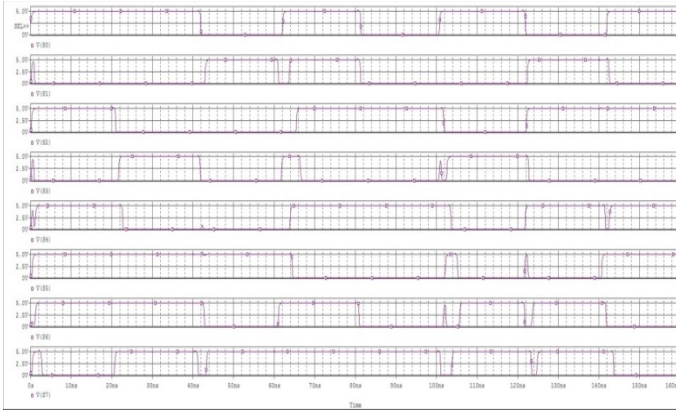

Fig. 6. Sum of the CMOS full adder

Table 1. Compare expected result with simulated result of CMOS full adder

Inputs		Outputs	
		Expected	Simulated
$A_7A_6A_5A_4A_3A_2A_1$	$B_7B_6B_5B_4B_3B_2B_1$	$S_7S_6S_5S_4S_3S_2S_1$	$S_7S_6S_5S_4S_3S_2S_1$
00011110	01010111	01110101	01110101
01010110	10010011	11101001	11101001
00110111	01101011	10100010	10100010
11110001	11100110	11010111	11010111
11100100	10110000	10010100	10010100
00101100	10011101	11001001	11001001
01001101	10001001	11010110	11010110
01010010	11100011	00110101	00110101

From the Figures 4-6 and Table 1 above, we can see all the inputs and outputs traces are correct. Fig. 7 shows the power consumption of the 8-bit traditional CMOS full adder.

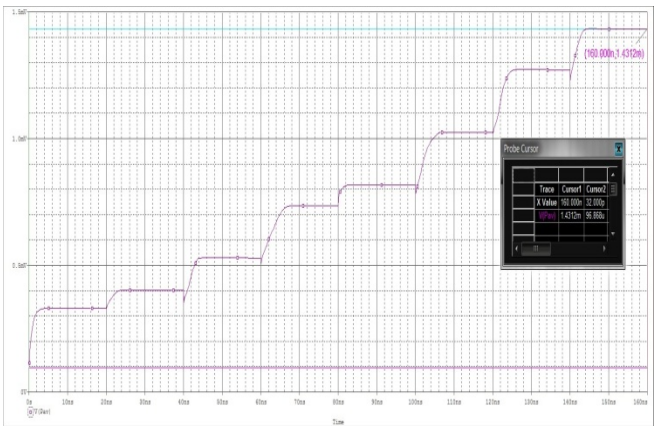

Fig. 7. Power dissipation of traditional full adder

From the image above we can see the power consumption of the designed 8-bit CMOS full adder design for the given input pattern sequence is P_{avg}(CMOS)=1.4312mW.

III. Eight-bit Static Energy Recovery Full Adder (SERF) Design

The cell of static energy recovery full adder only use 10 transistors and it does not need inverted inputs. The design was inspired by the XNOR gate full adder design. The SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption, removing the P_{sc} variable (product of I_{sc} and voltage) from the total power equation. The charge stored at the load capacitance is reapplied to the control gates.

This circuit operates well at higher supply voltages, but if the supply voltage is scaled to voltages lower than 0.3V, this circuit fails to work. This is confronted with some problems especially when the SERF adder at lower supply voltage. Assume that one of the two patterns ABC_{in}= '110' and '111' are applied. As seen from figure 8, when A=1 and B=1, the voltage at node F is V_{dd}-V_{th}. Now if the Cin is '0' then C_{out} will be equal to V_{dd}-$2V_{th}$ and the sum signal will go to zero. When C_{in}=1, C_{out} is connected to V_{dd} (may be lower) and the SUM signal is going to V_{dd}-V_{th}. Another problem with this circuit is when the floating node is connected to 0 (A=0, B=1 or A=1, B=0). When C_{in}=1, C_{out} is connected to V_{dd}, but if C_{in} is '0', C_{out} will be discharged to ground by a PMOS pass transistor that cannot fully discharge the output.

The design of 1-bit SERF adder [19] is shown in figure 8.

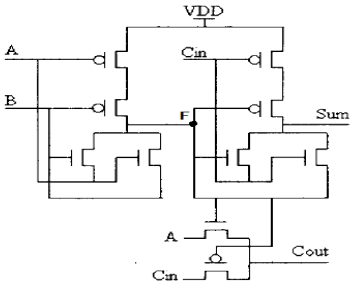

Fig. 8. Static Energy-Recovery Full (SERF) Adder (10 transistors) [19]

We also use PSPICE and hierarchical design to build the 1-bit and 8-bit SERF adder circuits. The PSPICE schematic design of 1-bit SERF adder is shown in Fig. 9. After it is designed and the function of the 1-bit SERF adder is verified to be correct with PSPICE simulation, the 1-bit SERF adder is defined as a block. In higher hierarchy level, it can be directly utilized without being implemented again. This greatly increase the efficiency of the design process. The PSPICE hierarchy design of the 8-bit energy recovery SERF adder is shown in Fig. 10.

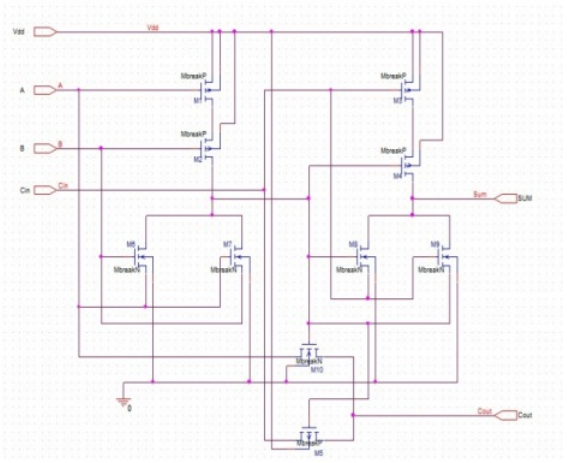

Fig 9. 1-bit SERF adder

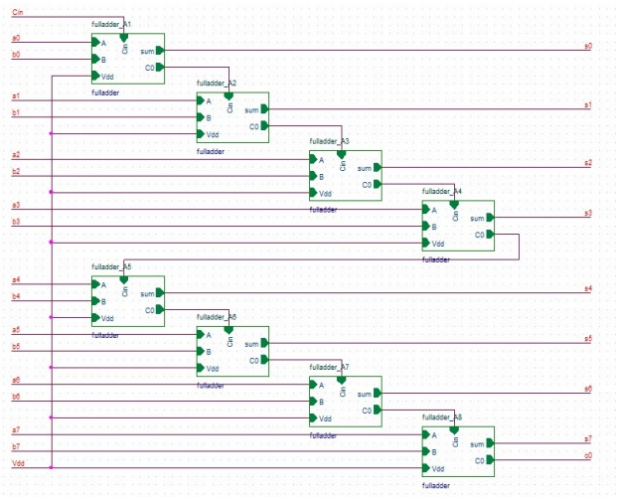

Fig. 10. PSPICE hierarchy design of 8-bit energy recovery SERF adder

The SERF adder only uses 10 transistors in each cell, so the total number of transistors in the 8-bit SERF adder is 80. Compared with the transistor count (224) of 8-bit CMOS full adder, the transistor count saving of 8-bit SERF adder is:

$$N_{save}=(224-80)/224\times100\%=64.3\% \quad (1)$$

Transistor count is a good estimation of circuit area. This indicates that the SERF energy recovery adder has smaller circuit area compared to CMOS design. That is, SERF energy recovery full adder is more area efficient.

To compare with the traditional adder, we use the same inputs patterns as CMOS full adder. The input patterns are shown in Fig. 4 and Fig. 5. After PSPICE simulation, the output SUM signal of 8-bit SERF adder is shown in Fig. 11 below.

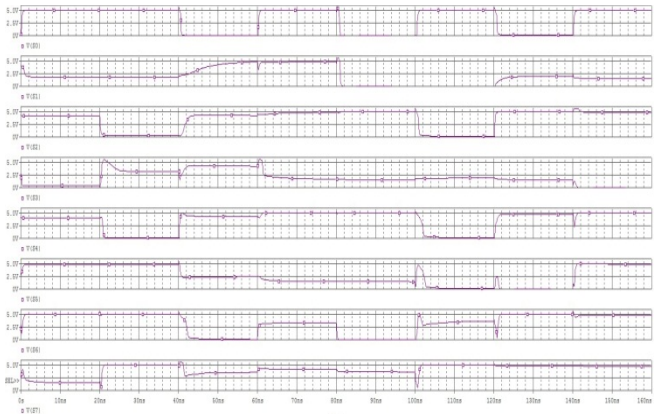

Fig. 11. PSPICE simulation curves of Sum of 8-bit SERF adder

Table 2. Compare expected result with simulated result of 8-bit SERF adder

Inputs		Outputs	
		Expected	Simulated
$A_7A_6A_5A_4A_3A_2A_1$	$B_7B_6B_5B_4B_3B_2B_1$	$S_7S_6S_5S_4S_3S_2S_1$	$S_7S_6S_5S_4S_3S_2S_1$
00011110	01010111	01110101	01110101
01010110	10010011	11101001	11101001
00110111	01101011	10100010	10100010
11110001	11100110	11010111	11010111
11100100	10110000	10010100	10010100
00101100	10011101	11001001	11001001
01001101	10001001	11010110	11010110
01010010	11100011	00110101	00110101

In above figure and table, we can see that the Sum of the 8-bit SERF adder is correct. However, for some patterns, we observe reduced voltage levels of the output voltages. Level restorer circuit may be introduced to recover the logic level to the expected values. PSPICE power simulation is also performed on the designed 8-bit SERF energy recovery full adder with the same pattern sequence as used for 8-bit CMOS full adder. The power simulation curve of the 8-bit SERF energy recovery full adder is shown in Fig. 12.

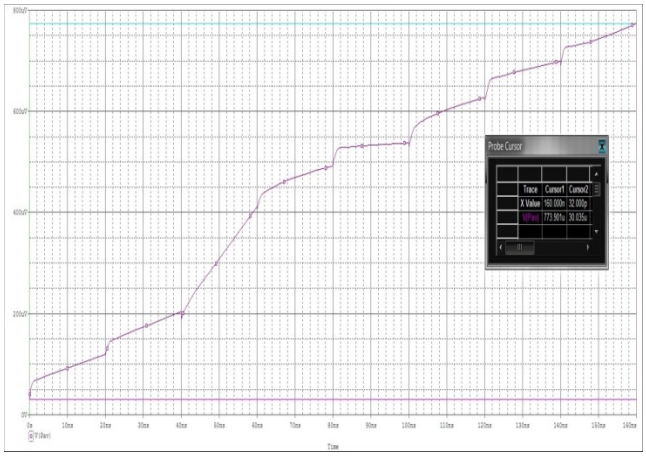

Fig. 12. PSPICE power simulation curve of 8-bit SERF energy recovery full adder

From Fig. 12, we can see the power consumption of the designed 8-bit SERF energy recovery full adder for the given input pattern sequence is P_{avg}(SERF)=773.901μW. Compared to the 8-bit static CMOS full adder (P_{avg}(CMOS)=1.4312mW), the average power of the 8-bit SERF adder is greatly reduced. The relative power saving of the 8-bit SERF energy recovery full adder compared to the CMOS adder is:

$$\text{Psave}=(1431.2\mu W - 773.901\mu W)/1431.2\mu W \times 100\% = 45.9\% \quad (2)$$

That is, for the given input pattern sequence, 8-bit SERF energy recovery full adder saves 45.9% power compared to CMOS design. This verifies the SERF energy recovery design is more power efficient than CMOS design.

IV. Conclusions and Future Work

In this paper, the design and simulation of an 8-bit SERF adder with PSPICE is proposed. In order for comparison, an 8-bit CMOS full adder is also designed. The total number of transistors used in CMOS full adder and SERF adder are 224 and 80. The 8-bit SERF energy recovery full adder saves 64.3% in transistor count than CMOS full adder design. For the given input pattern sequence, 8-bit SERF energy recovery full adder leads to 45.9% power saving compared to CMOS design. This shows that SERF adder uses less space and has lower power consumption than static CMOS adder. This makes the energy-recovery technique a promising candidate for low power design. In the future work, we will further use the energy recovery technique to other circuit, such as multiplier, ALU, etc.

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