2025 ASEE Northeast Section Conference, March 22, 2025, University of Bridgeport, Bridgpeort, CT, USA.

Realization of Optimized Adders for Power Efficient Applications

Suparshya Babu Sukhavasi
Electrical and Computer Engineering,
University of New Haven, Connecticut, USA
ssukhavasi@newhaven.edu

Sriphanindra Perali
Electrical Engineering
University of New Haven, Connecticut, USA
spera8@unh.newhaven.edu

Susrutha Babu Sukhavasi
Electrical and Computer Engineering,
Wentworth Institute of Technology, Boston,
Massachusetts, USA
sukhavasis@wit.edu

Sneha Gundeboyena
Electrical Engineering
University of New Haven, Connecticut, USA
sgund29@unh.newhaven.edu

Marisha Rawlins
Electrical and Computer Engineering,
Wentworth Institute of Technology,
Boston, Massachusetts, USA
rawlinsm@wit.edu

Abstract **– The study focuses on developing an efficient, customized full adder circuit using 2x1 multiplexers to address VLSI design's delay and power consumption issues. Traditional adders suffer from high propagation delays and power dissipation, limiting their efficiency in digital systems. By leveraging the efficiency of multiplexers, the proposed design achieves improved power efficiency and reduced delays compared to conventional gate-based adders. Multiplexers offer superior area efficiency, reduced transistor count, and simplified logic implementation, making them ideal for low-power and high-performance applications in VLSI systems. The research includes the design and detailed analysis of different adder architectures, including Ripple Carry Adder, Carry Look-Ahead Adder, and Carry Skip Adder, demonstrating the advantages of multiplexer-based adders in achieving low power dissipation and minimal delays. The findings highlight the effectiveness of multiplexer-based approaches in optimizing digital circuit performance, providing valuable insights for VLSI designers. Overall, this study advances VLSI technology by presenting an innovative approach to full adder design, enhancing power efficiency and performance while paving the way for future low-power design methodologies.**

Keywords- 2-bit Multiplexer, Full Adder, Low Power Design, Ripple Carry Adder, Carry Look-Ahead Adder, Carry Skip Adder, Delay, Power Dissipation, Area-LUT.

I. INTRODUCTION

In modern Very Large-Scale Integration (VLSI) design, arithmetic circuits play a crucial role in determining the performance, power efficiency, and area utilization of digital systems. Among these circuits, the full adder is a fundamental building block used in microprocessors, digital signal processing (DSP) units, and application-specific integrated circuits (ASICs). As transistor scaling advances to deep submicron technology, optimizing power consumption and propagation delay in arithmetic circuits has become increasingly important. However, conventional full adder designs exhibit limitations such as high propagation delays, excessive power dissipation, and increased transistor count, making them less efficient for energy-constrained applications [1], [2]. Traditional full adders are typically implemented using Complementary Metal-Oxide-Semiconductor (CMOS) logic, pass transistor logic (PTL), and transmission gates. In Ripple Carry Adders (RCAs), the sequential nature of carry propagation results in significant delays, making them unsuitable for high-speed applications [3]. Additionally, dynamic power dissipation due to frequent switching in conventional adder circuits is a major concern in low-power and battery-operated systems [4]. Another major limitation is the high transistor count, which leads to increased silicon area consumption, posing challenges in nanometer-scale integration [5]. These constraints necessitate exploring alternative adder architectures that achieve better trade-offs between speed, power, and area efficiency. To address these challenges, researchers have explored multiplexer (MUX)-based full adder designs, which offer reduced transistor count, lower propagation delay, and improved energy efficiency [6], [7]. A 2×1 multiplexer-based full adder significantly reduces the number of transistors required for sum and carry computation, leading to lower power consumption and enhanced area efficiency [8]. Due to these advantages, multiplexer-based adders are well-suited for power-constrained applications, including battery-powered devices, embedded systems, and AI accelerators [9]. Furthermore, MUX-based architectures provide better scalability, making them highly compatible with modern Field-Programmable Gate Arrays (FPGAs) and System-on-Chip (SoC) architectures [10]. This study proposes a customized full adder circuit using 2×1 multiplexers, focusing on power efficiency, delay reduction, and area optimization. The proposed design is evaluated against conventional Ripple Carry

Adder (RCA), Carry Look-Ahead Adder (CLA), and Carry Skip Adder (CSA) architectures, which are widely used in digital arithmetic operations [11]. The study further explores hybrid full adder designs, integrating pass transistor logic and CMOS techniques to further optimize performance. By analyzing these approaches, this research provides valuable insights for VLSI designers, semiconductor researchers, and chip architects working toward improving arithmetic logic units in high-performance computing, AI processing, and next-generation processors. In summary, this research presents an optimized full adder architecture leveraging 2×1 multiplexers, demonstrating significant improvements in power efficiency, propagation delay, and silicon area utilization compared to conventional adder designs. By exploring MUX-based methodologies, this study contributes to advancing low-power VLSI circuit design, offering an efficient and scalable solution for modern digital systems.

II. RELATED WORKS

The implementation of multiplexer-based adders has gained significant attention in VLSI design due to their efficiency in power consumption, reduced transistor count, and improved delay performance. Traditional full adders face challenges in terms of area utilization and power dissipation, which can be mitigated using multiplexer-based designs. Several studies have explored the benefits of employing 2-bit multiplexers in arithmetic circuits, focusing on optimizing performance for low-power applications. In [1], the design of 4-bit full adders was investigated using different logic styles, including CMOS, Pass Transistor Logic (PTL), and Transmission Gate Logic (TGL). The study compared power dissipation and delay, concluding that TGL-based designs exhibit superior power efficiency while maintaining minimal propagation delay. Similarly, from [2], a multiplexer-based low-power full adder architecture was proposed, demonstrating that an optimized multiplexer configuration leads to significant reductions in power consumption while maintaining computational accuracy. The study emphasized the critical role of transistor count in determining overall power efficiency, highlighting that PTL-based designs provide a balanced trade-off between delay and energy dissipation. In [3], the design of area-efficient and low-power multipliers utilizing multiplexer-based full adders was explored, showcasing how multiplexer logic reduces hardware complexity while improving computational efficiency, making them ideal for digital signal processing applications. Further, from [4], a low-power, high-speed 1-bit full adder circuit was presented at 45nm CMOS technology, showing that multiplexer-based full adders outperform conventional CMOS designs in terms of energy efficiency. The study concluded that multiplexer-based architectures effectively minimize switching activity and reduce overall circuit power dissipation. Additional research, such as [5], focused on designing multiplexer-based full adders for high-speed applications, demonstrating that integrating approximate computing techniques can further enhance energy efficiency in arithmetic circuits. From [6], a multiplexer-based carry-select adder was proposed, proving to be effective in optimizing speed while keeping power consumption minimal. Furthermore, [7] explored hybrid full adder designs incorporating MUX-based logic with dynamic power gating techniques, revealing promising results in reducing leakage power. These studies reinforce the effectiveness of using 2:1 multiplexers in arithmetic circuits, particularly in digital applications requiring low-power operation and compact hardware implementation. The comparative analysis of different logic styles indicates that multiplexer-based adders can achieve optimal results in power-sensitive applications, making them a promising alternative to conventional full adder designs. The findings from these studies support the methodology adopted in this work, where multiplexer-based adders are investigated for their potential in improving digital circuit efficiency. Efficient arithmetic operations are fundamental in digital circuits, particularly in applications requiring high-speed computation and low power consumption. The design of adders has evolved significantly to address the challenges of delay, power, and area efficiency. Among the various approaches, multiplexer (MUX)-based designs have gained popularity due to their simplicity and reduced transistor count. This section provides an overview of how adders are designed starting from the basic 2:1 multiplexer, progressing toward full adder implementations, and extending to multi-bit adders.

2.1 Basic 2-bit Multiplexer

A 2-bit multiplexer (MUX) is a fundamental combinational circuit that selects one of two inputs based on a control signal. The Boolean equation for a 2-bit MUX is:

$$Y = A \cdot S + B \cdot S'$$

where: A, B are the input signals, S is the select signal, Y is the output. This simple structure forms the basis for implementing various arithmetic circuits, including full adders and other logic functions.

2.2 Full Adder Using 2-bit MUX

A full adder adds three binary inputs: A, B, and Carry-in (Cin), producing a sum (S) and a carry-out (Cout). The sum and carry functions can be expressed using multiplexers as:

$$S = MUX(Cin, MUX(B, B', A), MUX(B', B, A))$$

$$Cout = MUX(A, B, Cin)$$

By implementing the above logic using only 2x1 MUX circuits, a full adder can be efficiently realized with fewer transistors compared to conventional CMOS logic-based implementations. A study in demonstrated that MUX-based full adders significantly reduce power dissipation and propagation delay, making them an attractive choice for low-power VLSI applications. Once a single-bit full adder is implemented using multiplexers, it can be cascaded to construct 4-bit, 8-bit, and 16-bit adders. The design choices for multi-bit adders are discussed below.

2.3 Higher Bit Adders Using MUX-Based Full Adders

A 4-bit adder consists of four MUX-based full adders connected in series, where the carry-out of each stage propagates to the next stage as carry-in. This architecture is functionally similar to a Ripple Carry Adder (RCA) but with optimized power and delay characteristics due to the MUX-based implementation. By replacing conventional XOR-based sum and AND-OR-based carry with MUX-based logic improves power efficiency without significantly increasing area overhead. For higher-bit adders, using a simple Ripple Carry Adder (RCA) structure becomes inefficient due to the increased propagation delay. To address this, various optimized architectures have been proposed such as Carry Skip Adder (CSA) reduces delay by skipping redundant carry computations. Carry Lookahead Adder (CLA) Uses generate (G) and propagate (P) logic to speed up carry generation. A comparison in confirms that 16-bit adders require additional optimization techniques, such as to maintain speed efficiency.

III. PROPOSED CIRCUIT DESIGN

The primary objective of this study is to develop an optimized adder architecture that balances speed, power consumption, and area efficiency for VLSI applications. This section details the Ripple Carry Adder (RCA), Carry Lookahead Adder (CLA), and Carry Skip Adder (CSA) implementations using the MUX-based approach. The circuit diagrams presented are based on hardware descriptions synthesized and verified in FPGA/VLSI environments.

3.1 Ripple Carry Adder (RCA)

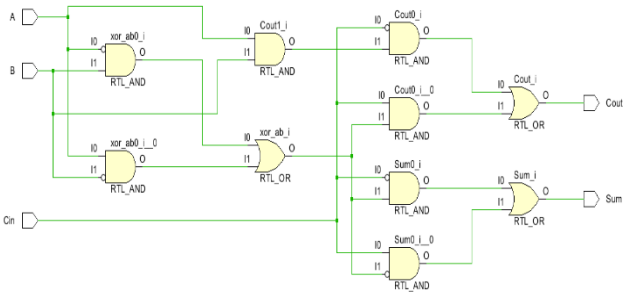
The Ripple Carry Adder (RCA) is the most straightforward adder architecture, where the carry-out (Cout) of each stage propagates to

the next stage sequentially. The logic equations for Sum and Carry for a single-bit full adder are:

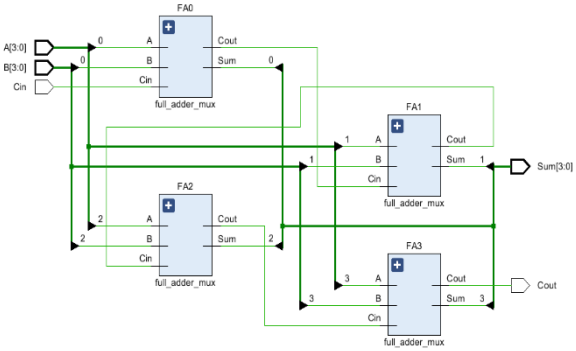
$$Sum = A \oplus B \oplus Cin$$
$$Cout = (A \cdot B) + (Cin \cdot (A \oplus B))$$

Circuit Diagram (RCA)

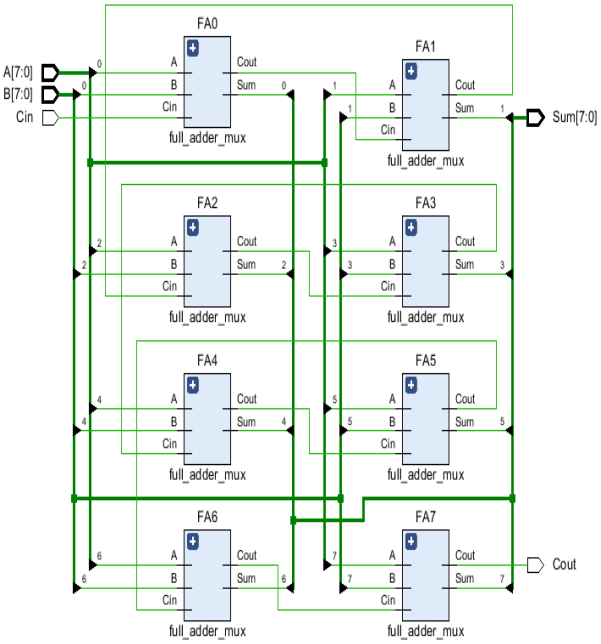
The hardware implementation of RCA, synthesized using Verilog, produces the following RTL-level schematic:



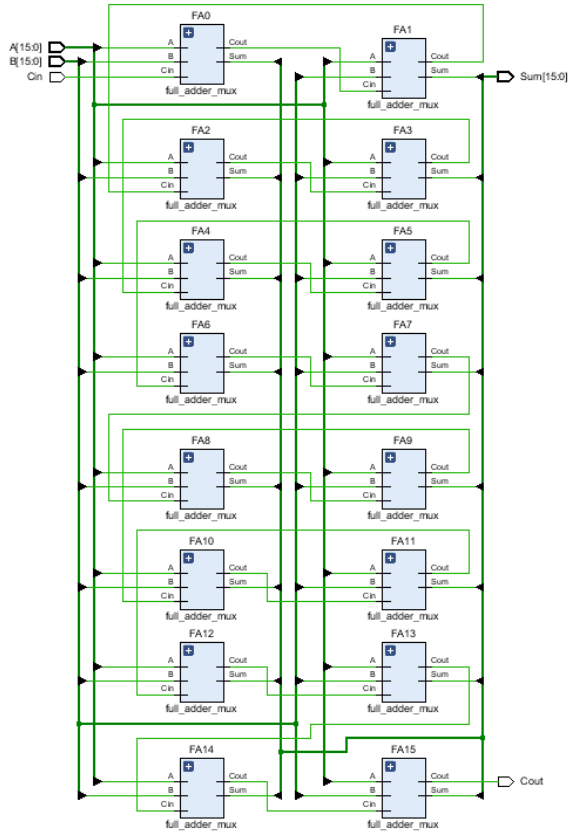
(a)



(b)



(c)



(d)

Figure 1: (a) 1-bit Ripple Carry Adder (b) 4-bit Ripple Carry Adder (c) 8-bit Ripple Carry Adder (d) 16-bit Ripple Carry Adder

Design Observations

Simple structure with low area utilization. High propagation-delay due to sequential carry generation. Power consumption increases with bit-width.

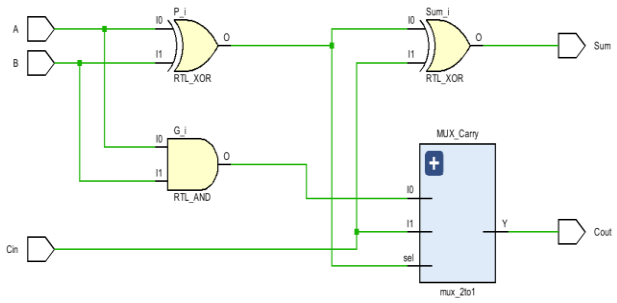
3.2 Carry Lookahead Adder (CLA)

To address the delay bottleneck in RCA, the Carry Lookahead Adder (CLA) computes carry bits in advance using Generate (G) and Propagate (P) signals:

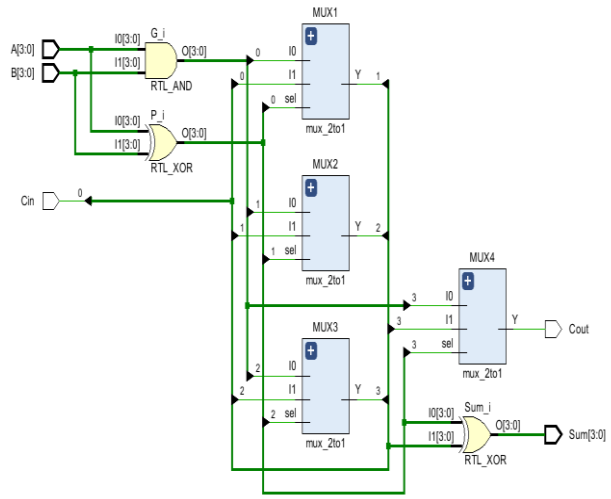
$$Gi = Ai \cdot Bi$$
$$Pi = Ai \oplus Bi$$
$$Ci + 1 = Gi + (Pi \cdot Ci)$$

Circuit Diagram (CLA)

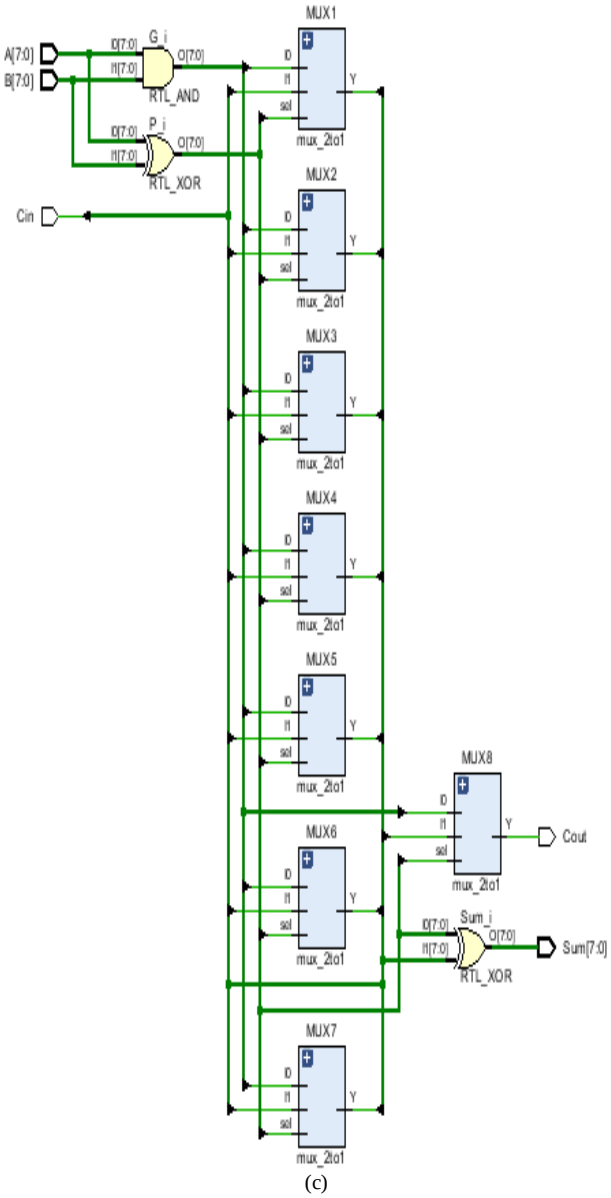
The hardware implementation of CLA produces the following optimized carry computation circuit:



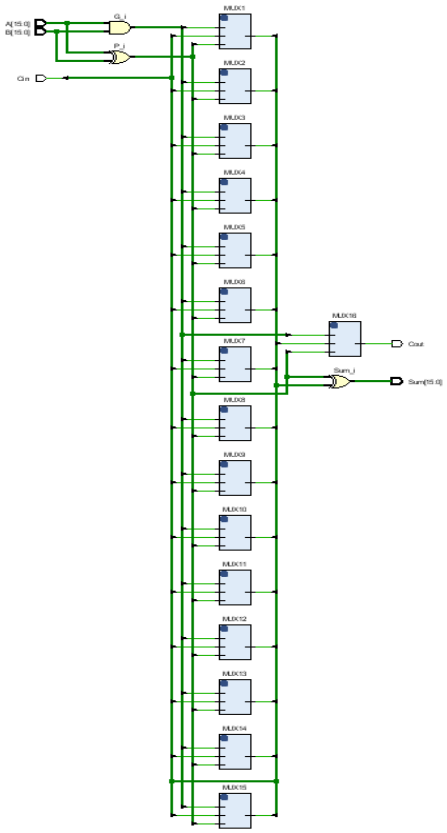
(a)



(b)



(c)



(d)

Figure 2: (a)1-bit Carry Lookahead Adder (b)4-bit Carry Lookahead Adder (c) 8-bit Carry Lookahead Adder (d) 16-bit Carry Lookahead Adder

Design Observations

Faster carry computation, reducing overall propagation delay. Increased hardware complexity due to additional logic gates. More power consumption than RCA due to extra generate-propagate computations.

3.3 Carry Skip Adder (CSA)

The Carry Skip Adder (CSA) enhances speed by reducing the propagation delay caused by sequential carry computation in a traditional Ripple Carry Adder (RCA). It works by grouping bits into blocks and allowing the carry signal to skip over multiple adder stages when certain conditions are met, significantly reducing overall computation time. The CSA achieves this by using a carry propagation (P) signal, which determines whether the carry should be forwarded to the next stage immediately or be computed sequentially.

Mathematical Representation

The carry propagation (P) for a block of adders is given by:

$$P = P0 \cdot P1 \cdot P2 \cdots Pn$$

where Pi is the propagate signal for each bit and is defined as:

$$Pi = Ai \oplus Bi$$

If **P = 1**, the carry can be skipped over the block; otherwise, it must propagate sequentially. The carry-out equation for a single-bit full adder within a block is:

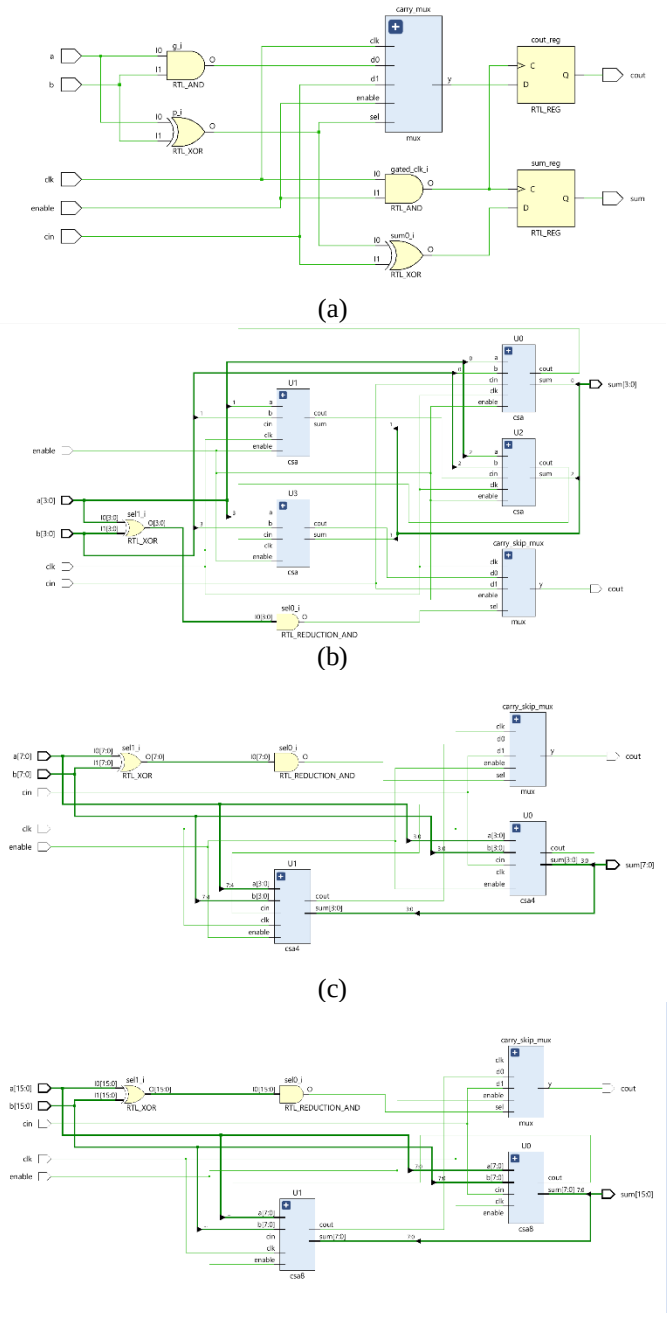
$$Ci + 1 = Gi + (Pi \cdot Ci)$$

where: **Gi** (Generate signal) = Ai·Bi; **Pi** (Propagate signal) = Ai⊕Bi; **Ci** is the carry-in of the stage. For multi-bit blocks, the carry-skip logic optimizes carry propagation:

$$Cout = Cin + P \cdot (Cin - Cin - 1)$$

Circuit Diagram (CSA)

The hardware implementation of the CSA, synthesized using Verilog, produces the following optimized carry skip logic circuit:



(a) (b) (c) (d)

Figure 3: (a) 1-bit Carry Skip Adder (b) 4-bit Carry Skip Adder (c) 8-bit Carry Skip Adder (d) 16-bit Carry Skip Adder.

Design Observations

Improves computation speed by skipping unnecessary carry propagation. Uses propagate logic to minimize sequential delay. Optimized power and area efficiency, making it suitable for large-bit-width operations. Balances performance between speed and hardware complexity, making it more efficient than RCA in delay and lower power than CLA.

IV. RESULTS AND DISCUSSION

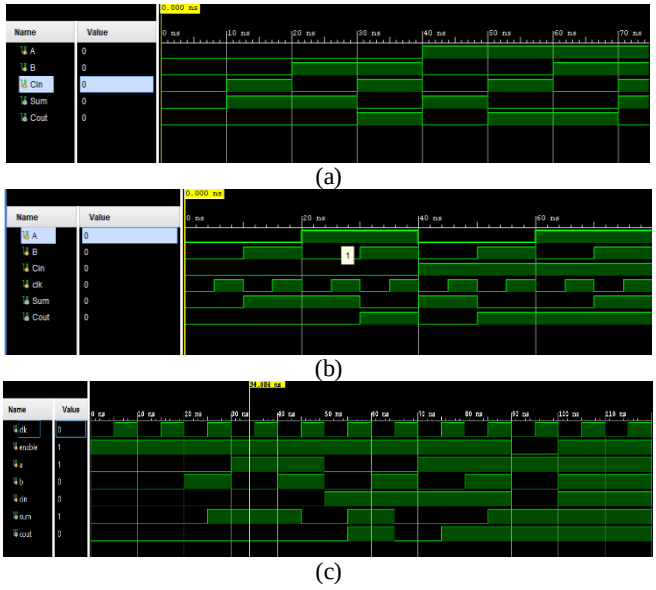
Presenting the simulation results, waveforms, and comparative performance metrics of the proposed multiplexer-based adder architectures, including Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), and Carry Skip Adder (CSA). The performance evaluation is based on logic delay, power consumption, and area utilization (LUTs) for 1-bit, 4-bit, 8-bit, and 16-bit adders.

4.1 Simulation Results

The provided waveform simulations illustrate the correct functionality and performance analysis of the proposed MUX-based adder architectures. Each simulation verifies the sum and carry outputs for different input conditions.

A. 1-Bit Adder Waveforms

The 1-bit RCA, CLA, and CSA designs were simulated in Vivado.
Input signals include A, B, and Cin.
Outputs: Sum and Carry-out (Cout).
The MUX-based 1-bit adder demonstrates lower propagation delay than conventional CMOS-based full adders.

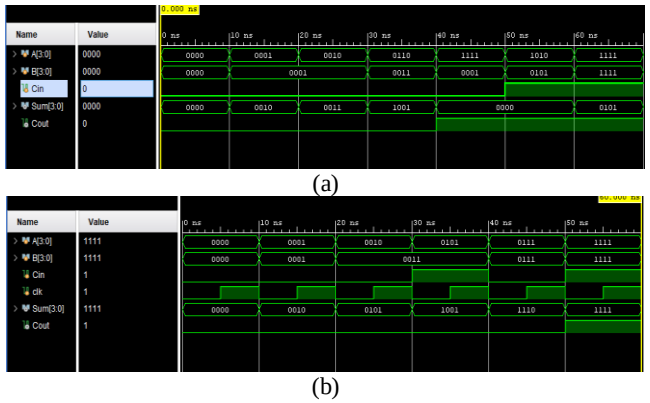


(a) (b) (c)

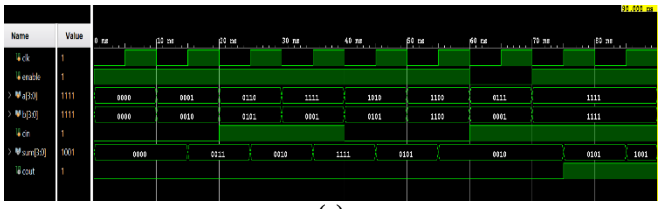
Figure 4: Timing waveforms of (a) 1-bit Ripple Carry Adder (b) 1-bit Carry Lookahead Adders (c) 1-bit Carry Skip Adder

B. 4-Bit Adder Waveforms

4-bit RCA suffers from sequential carry propagation, leading to higher delay. CLA and CSA improve speed by utilizing carry-lookahead and skip logic. MUX-based CLA & CSA achieve better power efficiency compared to standard CMOS implementations.



(a) (b)

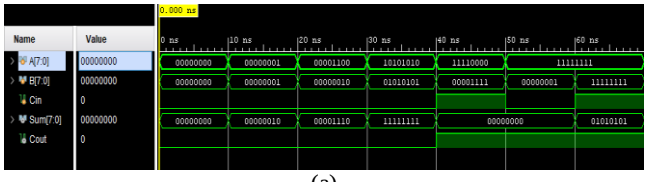


(c)

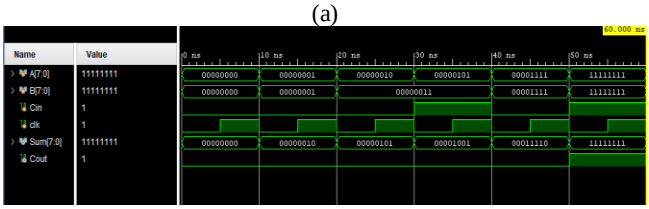
Figure 5: Timing waveforms of (a) 4-bit Ripple Carry Adder (b) 4-bit Carry Lookahead Adders (c) 4-bit Carry Skip Adder

C. 8-Bit Adder Waveforms

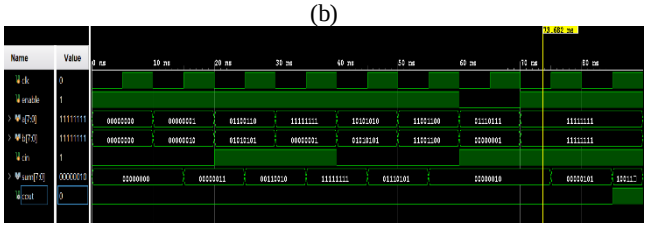
8-bit RCA further suffers from increased carry propagation delay. CLA and CSA provide faster computation at the cost of slightly higher power consumption. The MUX-based implementation optimizes power and area utilization.



(a)



(b)

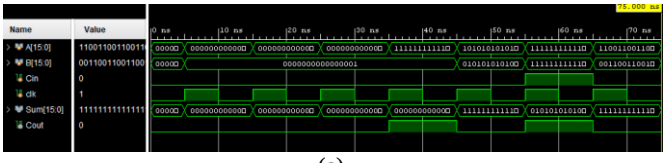


(c)

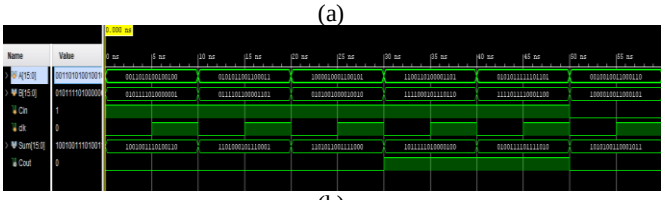
Figure 6: Timing waveforms of (a) 8-bit Ripple Carry Adder (b) 8-bit Carry Lookahead Adders (c) 8-bit Carry Skip Adder

D. 16-Bit Adder Waveforms

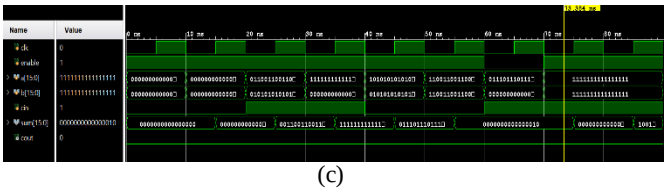
The 16-bit RCA has significant propagation delay, making it unsuitable for high-speed applications. CLA and CSA provide enhanced computational efficiency while minimizing power dissipation. The MUX-based design effectively reduces transistor count, lowering power consumption and silicon area utilization.



(a)



(b)



(c)

Figure 7: Timing waveforms of (a) 16-bit Ripple Carry Adder (b) 16-bit Carry Lookahead Adders (c) 16-bit Carry Skip Adder

4.2 Comparative Analysis of RCA, CLA, and CSA

The performance of RCA, CLA, and CSA architectures is evaluated across multiple metrics. Based on the simulation results:

A. Logic Delay:

Logic Delay (ns)			
No.of Bits	RCA	CLA	CSA
1-bit	3.42	3.28	2.76
4-bit	3.61	3.59	2.7
8-bit	4.01	4.02	2.8
16-bit	4.53	4.53	1.28

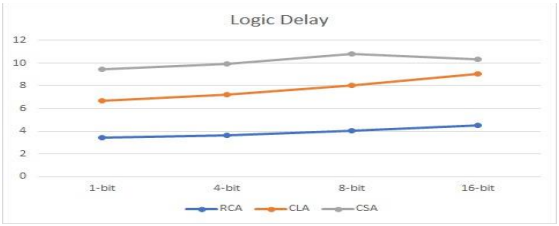


Figure 8. Delay

CLA exhibits the lowest delay due to parallel carry computation. RCA has the highest delay, making it unsuitable for high-speed applications. CSA provides a middle-ground with reduced carry propagation time.

B. Area Utilization (LUT Count):

Area/LUT (%)			
No.of Bits	RCA	CLA	CSA
1-bit	1	2	1
4-bit	4	5	3
8-bit	8	8.7	8
16-bit	16	16.71	12

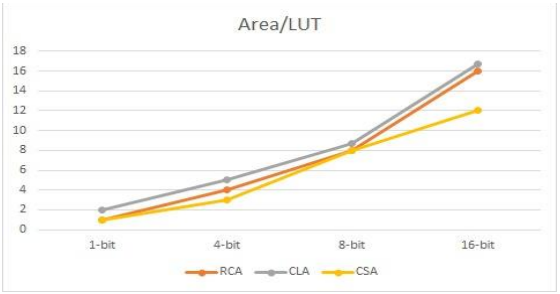


Figure 9: Area Utilization

RCA uses minimal hardware resources but suffers from slow performance; CLA requires more LUTs but significantly improves computation time; CSA maintains moderate LUT usage while enhancing speed and efficiency.

C. Power Consumption:

Power Report (mW)			
No.of Bits	RCA	CLA	CSA
1-bit	1	1	1
4-bit	3	3	3
8-bit	6	5	6
16-bit	13	11	10

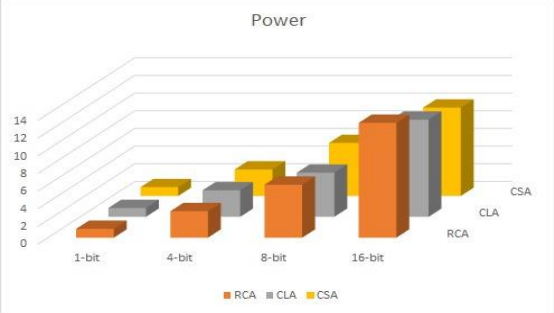


Figure 10: Power Chart

Multiplexer-based designs show reduced power dissipation compared to traditional gate-based implementations. CLA consumes more power due to additional logic units for parallel processing.CSA balances power efficiency and speed. The bar charts illustrate the performance comparison of 1-bit, 4-bit, 8-bit, and 16-bit adders in terms of area, power, and logic delay, demonstrating that multiplexer-based adders provide an optimal balance for low-power, high-performance applications.

4.3 Discussion

Ripple Carry Adder (RCA) is area-efficient, it suffers from sequential carry propagation, leading to higher logic delay, making it unsuitable for high-speed applications. Carry Look-Ahead Adder (CLA) significantly reduces delay by using generate-propagate logic, but it comes at the cost of higher area utilization and slightly increased power consumption. Carry Skip Adder (CSA) provides a balanced trade-off between speed and area, making it suitable for applications requiring moderate power efficiency and high speed. Usage of MUX-Based Full Adder Optimization improves power efficiency and reduces transistor count, making it highly beneficial for battery-operated devices and AI accelerators. After designing the proposed full adder, simulations were performed to evaluate its power efficiency, propagation delay, and area utilization. The study primarily focuses on dynamic power dissipation, which is a key concern in low-power VLSI design. However, leakage power is also a critical factor, especially in deep submicron technologies, where static power consumption significantly impacts overall efficiency. While leakage power analysis was not included in this phase, it will be thoroughly examined in future work through layout-level simulations and transistor-level optimizations to ensure comprehensive low-power design improvements. The proposed design was evaluated for 1-bit, 4-bit, 8-bit, and 16-bit adders to analyze improvements in power efficiency, propagation delay, and area utilization. While larger architectures such as 32-bit and 64-bit adders were not implemented in this study, performance trends suggest that propagation delay would increase due to carry chain dependency, particularly in Ripple Carry Adders (RCAs). As the adder size increases from 1-bit to 16-bit, the overall power consumption tends to rise due to an increase in the number of switching transistors. This is primarily influenced by dynamic power dissipation, which depends on switching activity, capacitance, and operating frequency. However, multiplexer-based adders benefit from a lower transistor count, leading to better power efficiency compared to traditional CMOS-based adders. For higher-bit adders (32-bit and 64-bit), the power impact can be analyzed in two aspects:

1) Dynamic Power: Since power is proportional to the number of switching events, a larger number of logic stages results in higher dynamic power dissipation. This effect is more prominent in Ripple Carry Adders (RCAs) due to sequential carry propagation.
2) Leakage Power: As transistors increase in higher-bit architectures, leakage power becomes a significant factor, especially in deep submicron technologies where static power consumption grows due to subthreshold leakage currents.

While our current study focuses on 1-bit to 16-bit adders, the power consumption trend suggests that multiplexer-based adders will still offer reduced dynamic power and better energy efficiency in higher-bit architectures. Future work will include layout-level power analysis to quantify dynamic and leakage power effects in 32-bit and 64-bit implementations, optimizing the design for scalability and low-power VLSI applications. .However, multiplexer-based logic could still provide advantages in power efficiency and reduced transistor count compared to conventional designs. Future work will focus on scalability analysis for higher-bit architectures to optimize delay and power trade-offs while ensuring efficient implementation in complex digital processors.

4.4 Application in AI and Embedded Systems:

Multiplexer-based adders are highly suitable for AI accelerators, embedded processors, and cryptographic circuits, where power efficiency, low latency, and area optimization are critical factors. In AI accelerators, particularly in Deep Learning Processors (DLPs) and Tensor Processing Units (TPUs), arithmetic operations such as MAC (Multiply-Accumulate) and convolutional computations require fast and energy-efficient adders [8]. The reduced transistor count, and lower power dissipation of multiplexer-based adders make them well-suited for high-performance AI workloads, enabling lower power consumption in battery-operated AI devices [10]. For embedded processors, power efficiency is a primary design constraint, especially in IoT (Internet of Things) devices, wearable electronics, and low-power edge computing platforms. Multiplexer-based adders, with their optimized switching activity and reduced leakage power, contribute to extending battery life and enhancing processing efficiency in these resource-constrained environments [2]. Additionally, in cryptographic circuits, such as those used in AES (Advanced Encryption Standard) and RSA (Rivest–Shamir–Adleman) encryption algorithms [21], arithmetic units need to handle large-bit operations efficiently. The low-power characteristics of multiplexer-based adders make them advantageous for hardware security modules (HSMs) and encryption processors, where minimizing power leakage is essential to prevent side-channel attacks [9]. Thus, by improving power efficiency, delay reduction, and area utilization, multiplexer-based adder designs enhance the performance of AI accelerators, embedded processors, and cryptographic hardware, making them a viable solution for next-generation low-power computing applications.

V. CONCLUSION

Presenting an optimized full adder architecture using 2×1 multiplexers, effectively addressing power dissipation, propagation delay, and area utilization challenges in conventional CMOS-based

adders. By integrating MUX-FA logic into RCA, CLA, and CSA architectures, the study demonstrates significant improvements in computational speed and power efficiency. The proposed approach is highly beneficial for low-power, high-speed digital computing applications, including AI accelerators, embedded systems, and high-performance processors. Future work will explore further hybrid implementations incorporating dynamic power gating techniques and approximate computing strategies to optimize adder performance for ultra-low power applications.

REFERENCES

[1] Rachana Dayall, Deepak Kumar, "Multiplexer-Based Design of Adders for Low Power VLSI Applications," *International Research Journal of Engineering and Technology (IRJET)*, Vol. 07, Issue 06, June 2020.

[2] Nischitha K, K. B. Ramesh, "Multiplexer-Based Design of Adders for Low Power VLSI Applications," *International Research Journal of Modernization in Engineering Technology and Science*, Vol. 04, Issue 02, February 2022.

[3] S. Murugeswari and S. K. Mohideen, "Design of area-efficient and low-power multipliers using multiplexer-based full adder," *Second International Conference on Current Trends In Engineering and Technology - ICCTET 2014*, 2014.

[4] A. K. Yadav, B. P. Shrivatava, and A. K. Dadoriya, "Low power high-speed 1-bit full adder circuit design at 45nm CMOS technology," *2017 International Conference on Recent Innovations in Signal Processing and Embedded Systems (RISE)*, Bhopal, India, 2017.

[5] Mukherjee and A. Ghosal, "Design & study of a low power high-speed full adder using GDI multiplexer," *2015 IEEE 2nd International Conference on Recent Trends in Information Systems (ReTIS)*, 2015, pp. 465-470.

[6] S. Jain, S. Rawat, P. Chaturvedi, and M. Kapoor, "VLSI Architecture for Low Cost and Power Reversible Arithmetic Logic Unit based on Reversible Gate," *2018 International Conference on Advanced Computation and Telecommunication (ICACAT)*, 2018.

[7] P. Sadhasivam and M. Manikandan, "Low area and high-speed confined multiplier using multiplexer-based full adder," *Second International Conference on Current Trends In Engineering and Technology - ICCTET 2014*, 2014.

[8] Y. Shanmugam, S. Chandran, C. Rohith, and R. Silambarasan, "Design and Analysis of Approximate Adders Using Multiplexer," *2021 7th International Conference on Advanced Computing and Communication Systems (ICACCS)*, Coimbatore, India, 2021.

[9] R. Singh and A. Kumar, "Design and analysis of a low power high-speed full adder using 2×1 multiplexer," *2022 IEEE North Karnataka Subsection Flagship International Conference (NKCon)*, Vijaypur, India, 2022.

[10] P. Bajpai, P. Mittal, A. Rana, and B. Aneja, "Performance analysis of a low power high-speed full adder," *2017 2nd International Conference on Telecommunication and Networks (TEL-NET)*, Noida, India, 2017.

[11] N. A. Kamsani, V. Thangasamy, S. J. Hashim, Z. Yusoff, M. F. Bukhori, and M. N. Hamidon, "A low power multiplexer-based pass transistor logic full adder," *2015 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)*, Kuala Terengganu, Malaysia, 2015.

[12] S. Radhakrishnan, T. Nirmalraj, R. K. Karn and S. K. Pandiyan, "Low latency power aware self-checking based CSA for sequential multiplier," *2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI)*, 2017, pp. 1056-1059, doi: 10.1109/ICPCSI.2017.8391872.

[13] X.Sun, J.Feng, "A 10 Gb/s Low-power 4:1 Multiplexer in 0.18μm CMOS,"*Proceedings of International Symposium on Signals, Systemsand Electronics (ISSSE2010)*, 2010.

[14] R. V. Anugraha, D. S. Durga and R. Avudaiammam, "Design and performance analysis of 2:1 multiplexer using multiple logic families at 180 nm technology," *2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, Bangalore, India, 2017.

[15] M. Agarwal, N. Agrawal and M. A. Alam, "A new design of low power high speed hybrid CMOS full adder," *2014 International Conference on Signal Processing and Integrated Networks (SPIN), Noida, India*, 2014, pp. 448-452, doi: 10.1109/SPIN.2014.

[16] Mohammed Zeeshan A, Kiran V. Design and comparison of full adder using TG Based 4:1 MUX. *International Journal of Research and Review. 2022*; 9(11): 91-95.

[17] Vikash Kumar Sharma, Dr. Shyam Akashe," Power Efficient Design of 4:1 Multiplexer usingLow Power Techniques", *International Journal of Modern Engineering & Management Research* | Vol 4 | Issue 4 | Dec 2016.

[18] Ram Singh, Amit Kumar, "Design and analysis of a low power high speed full adder using 2×1 multiplexer", *2022 IEEE North Karnataka Subsection Flagship International Conference (NKCon)*, pp.1-7, 2022.

[19] N. Divya, G. Ilakkiya, M. Dheeraj, R. Hinduja, M. Gokul Nathan, M. Harish, "Design and Implemetation of Combinational Logic Circuits using Open Source Tool", *2022 International Conference on Automation, Computing and Renewable Systems (ICACRS)*, pp.82-87, 2022.

[20] Charu Chaudhary, Uma Sharma, "Exploring Diverse Logic Implementations and Full Adder Circuit Designs", *2024 International Conference on Electrical Electronics and Computing Technologies (ICEECT)*, vol.1, pp.1-6, 2024.

[21] Sukhavasi, Susrutha Babu, Suparshya Babu Sukhavasi, Khaled Elleithy, and Abdelrahman Elleithy. "Analysis and implementation of proficient Rijndael algorithm with optimized computation." *IEEE Long Island Systems, Applications and Technology Conference (LISAT)*, pp. 1-5. IEEE, 2017.