RECONFIGURABLE LOGIC IN LABORATORY INSTRUCTION

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ABSTRACT:

Traditionally, laboratory instruction in computer and electronics engineering technology has relied mainly on SSI and MSI integrated circuits. This placed a limitation on the number of components per lab experiment, and hence, a limitation on the complexity of the laboratory tasks presented to students. Exasperated by the laboratory session's time duration and the methods available for circuit construction, circuits built as laboratory experiments are, more often than not, rather simple. Although possible, it is very difficult to perform complex testing on a proto-board. To allow for complex circuits to be designed and tested in a laboratory environment, a solution has been adopted here at the University of Southern Mississippi (USM). Namely, the use of reconfigurable circuit design techniques. Using reconfigurable logic, circuits with a high level of complexity may be designed, built, and tested by the students in a relatively short period of time. The hardware and software used at USM has been limited to Xilinx's and Altera's Field Programmable Gate Arrays (FPGAs) development tools running on a PC platform. The primary reason for using these manufacturers has been cost. Both Xilinx and Altera have donated software and hardware for the USM laboratories.

This paper will examine the methodology used to introduce the students to the concept of re-configurable logic, the use of this technology in the laboratory, and the impact of this technology on student learning. Finally, the advantages and disadvantages of this technology are outlined.

INTRODUCTION:

Today's market has a wide range of programmable electronic devices, starting with the PAL and GAL devices to FPGAs with tens of thousands of gates per IC. At the high end, the number of programmable elements per device has steadily been increasing. The level at which such devices are programmed has also been increasing, or becoming more user friendly. The ease by which these devices are programmed has prompted their incorporation in the CET curriculum at the University of Southern Mississippi. This has allowed the introduction of sophisticated lab experiments exposing the students to complex digital concepts.

The software package currently used in our course CET 472 (Sequential Circuits) is Foundation running under Xilinx. This package allows for the design of circuits using either Schematics, State Diagrams or HDL. The resulting design may be tested (simulated,) modified and downloaded to FPGA test boards realizing the circuit. The entire process is handled through a GUI running under Windows 95; therefore, very little time is used up in introducing students to this package. A single lab session that our students take at their sophomore year was found to be sufficient to introduce this package. Nevertheless, more training on this package with highly sophisticated designs are to be implemented.

FOUNDATION:

The Foundation Series software, used on Windows NT and Windows 95 PCs, is a complete, ready-to-use design package for Xilinx programmable logic devices. The software features easy-to-use graphical HDL (VHDL and Verilog) design tools, advanced synthesis and optimization technologies, and push-button design flows, enabling designers to produce expert HDL designs in minutes for Xilinx programmable logic devices. [3]

In addition to the broad acceptance of the Foundation Series software by the commercial market, Xilinx has partnered with Prentice Hall, the premier publisher of engineering books and software for the academic market, to promote the use of programmable logic and HDL methodologies in institutions of higher education. In December of 1997, Prentice Hall began shipping Xilinx Foundation Series Student Edition to academic bookstores worldwide for use in college-level instruction. The Xilinx Student Edition is available for student purchase only and includes the Foundation Series software, the "Practical Xilinx Designer" lab book (a step-by-step design tutorial,) and a discount coupon for FPGA and CPLD prototyping boards. [3]

HARDWARE REQUIREMENTS AND COST:

Both Altera and Foundation running under Xilinx have minimal computing power needs. A minimum of 486 with 8 Mega bytes of RAM is required. More realistically, a ‘586 or 686 with 32 Megs of RAM should be used. Increasing system’s RAM improves the performance greatly. Clearly the platform requirements are within the reach of all schools, leaving the software and FPGA hardware as the main obstacle. Fortunately, both Altera and Xilinx have aggressive university support programs that can go as far as full donation of software and hardware to universities.

More information on what is available, the cost and educational discounts may be found in the Xilinx home page at www.xilinx.com and for Altera at www.altera.com.

The cost of FPGA ICs runs from a few dollars to over $100. Again, university support can play a roll on the cost of these devices.

CHANGES IN LABORATORY EXPERIMENTS:

An example of the laboratory experiments was the design and testing of a Universal Asynchronous Receiver Transmitter. In this experiment the students were asked to design and build a UART capable of 8 bit words, two stop bits, and hand shaking. Although it took a complete lab session to explain design aspects of the UART. The actual designing and building of the UART was completed in a single laboratory session. The UART designed could supply the tri-stated status signals for data available and transmit buffer empty. The inputs to the UART were the 8 bi-directional data bus lines, a data strobe signal that signals the onset of transmission, and a receive data enable signal that allows the received data to drive the data bus. Letting students design such a system introduces them to a wide range of complex concepts. Problems such as timing of signals could be tested and the results of improper design could be verified. Although such a device is by no means taxing to the FPGA ICs used, namely the X4000, building such a design using MSI technology will be rather difficult.

Another laboratory experiment was to design and implement a traffic light controller. Such a design can be as simple as a timed signal intersection to one that could sense the presence of cars and act accordingly. To design an intelligent traffic light with 8 inputs and 8 outputs, the design process had to be automated. Even with the design process complete, the implementation phase could not be completed without the use of FPGAs. The reason for this being that the circuit required the use of over 20 flip-flops, two timers plus discrete logic. Although this experiment was done previously, it has always been treated as a project in which students were allowed to work in-groups and were allowed up to four weeks to complete the circuit. Again, using FPGAs the traffic light controller is now an experiment that each student has to complete individually in the span of two lab sessions.

The only drawback to using FPGAs in the educational setting is that they deprive the student from learning the circuit building and debugging techniques. Therefore, SSI and MSI ICs are still in use in introductory digital courses, and FPGAs are now used at the sophomore and junior levels.

CONCLUSIONS:

Reconfigurable logic technology and its support software have made the implementation of complex electronic designs rather simple. Although the designer still has to go through the normal design steps, the implementation of one’s design is no longer the tedious process of making and breaking connections. Rather, it is now the downloading of a bit file that would create the circuit on the reconfigurable IC. Furthermore, modifications to a circuit are as simple as downloading the modified bit file. The ease of use and the level of circuit complexity make this technology a good candidate for adoption in digital design laboratories.

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BIOGRAPHICAL INFORMATION:

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