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Research Experience for Community College Students: Design and Optimization of Non-Volatile Latch using Resistive Memory Technology

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Research Experience for Community College Students: Design and Optimization of Non-Volatile Latch using Resistive Memory Technology

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Abstract

Research experience is enriching and inspiring for undergraduate students. Early exposure to research experience is very effective in building interest and improving retention for students in STEM fields. Given the often-lengthy background preparation needed for conduct of research, it is difficult to incorporate research experience as a curricular activity in regular semesters when students have a lot of distractions managing various assignments in different courses. To address this challenge, we have developed summer research opportunities for community college students. Summer is a time when students have less distractions and can be effectively engaged in a focused research activity. The research internship is planned over 10 weeks of summer, and the student interns are assigned a graduate student mentor and a faculty advisor. This paper presents the details of this project, research and educational objectives, results obtained, and the student surveys assessing the outcomes. The planned research project is related to non-volatile resistive memory technologies, which are promising nano-scale technologies for information storage. In such technologies, the information is stored in a resistive form which is a state of a material that is non-volatile and also much more scalable as compared to the existing charge based storage technologies such as SRAM, DRAM, and flash. The main target application of resistive memory technologies is for large data storage and the main targeted market is replacement of computer DRAM main memory and SRAM cache. In this research, we propose a unique application for resistive memory technology and that is to realize non-volatile single-bit latch element that can be used for building reconfigurable logic circuits. The results of student surveys on the experience of student participants with the research internship strongly suggest that such an experience is very valuable in encouraging students to purse STEM research careers. Moreover, this experience enhances students' technical research skills such as scientific thinking, ability to analyze and interpret results, and presentation skills. This flipped approach to educational pathways in which research experience is offered early on results in students to be more determined and motivated as they progress through their educational pathways.

1. Introduction

The motivation behind this work was to offer research experience to undergraduate students and inspire them to pursue higher education and research careers. The main challenge of integrating

research experience in regular semesters is that students are already overwhelmed by many curricular activities that involvement in a focused research experience becomes very difficult to achieve. Moreover, offering meaningful research experience requires a significant level of preparation and support that may not be feasible to scale to a level accessible to a large number of students. An effective research experience for undergraduate students requires proper definition of a focused research problem, proper training and mentoring. Here we present a summer research program in which we host a selected group of students in a research lab for summer research experience and survey the impact of this experience on their educational outlook. Through a collaboration between a community college focused on education and a 4-year higher education institution offering research opportunities, we have been able to host four undergraduate students from the community college in our research laboratory in the 4-year university. The undergraduate student research interns were mentored by a master student who was experienced in the assigned research topic. A dedicated faculty member was in charge of defining and supervising the research tasks.

The research internship was conducted for ten weeks during summer. The undergraduate student interns had weekly meetings with their mentor and faculty advisor. The assigned research task was to explore design optimizations for a Non-Volatile Latch (NV-Latch) memory element using a resistive memory technology. The resistive memory technology considered was the emerging Spin-Transfer-Torque Magnetic Memory (STT-MRAM) technology. The research tried to evaluate the influence of various transistor sizing on area and power and performance trade-offs in the design. The end design goal was to come up with an optimal design which could achieve best performance and reliability under a given silicon area budget. The students were given orientation and resources to learn the basics of the spin-based electronics nanotechnology under investigation and the operation of the NV-Latch module. They were also given tutorials to learn the Spice circuit modeling and simulation. They were tasked to collect power, performance, and area results of various design points. They were then asked to interpret the results and offer meaningful conclusions as to the design optimization process and results achieved.

The students made midterm and final project progress report in both written and oral presentation forms to practice their wring as well as oral presentation skills. The students were surveyed on the effectiveness and satisfaction of their research experience before exiting the program. This paper shares the research project details, research results, and the student survey results.

2. Research Project Background: STT-MRAM Resistive Memory Technology

In this project, we optimized a Non-Volatile Latch (NV-Latch) that uses a resistive memory technology for achieving non-volatility. Compared to traditional computer memory, where information is stored as charge, resistive memory technology has information stored as a resistance state and hence it is non-volatile (i.e. the state is preserved even without power supply). The resistance state of the non-volatile cell is altered by a write driver, while a sense amplifier interprets the resistance of the non-volatile cell and sets the state of a volatile cell based upon that interpretation.

2.1 Non-Volatile Technology

Traditional memory storage systems that are used in almost all computer systems today rely on electric charges and charge levels to store information. Over time this charge can deteriorate and under sudden power failure be lost resulting in the permanent loss of information. Common examples of this include power outages, computers crashing, and batteries becoming faulty. The traditional method of storing memory is considered volatile memory as it can be lost very easily. The resistive memory technology offers a non-volatile method of information storage where the information is retained even if power is lost. The resistive memory used in this project is Spin-Transfer Torque RAM, STTRAM. In STTRAM, information is stored in the magnetic tunnel junction. The reason information cannot be lost with power loss is that it takes current to change the value of the data bit, which is determined by the magnetic/resistive state of the junction.

2.2 Magnetic Tunnel Junction: Non-Volatile Element in STT-MRAM

Magnetic Tunnel Junction or MTJ is a device that consists of a pinned or fixed magnetic layer—an insulating layer, which is the center of the device—and a free magnetic layer. The pinned layer, composed of a ferromagnetic substance such as Cobalt-Iron-Boron (CoFeB), generates a magnetic field that points only in one direction. The free layer, also made of CoFeB, can point either in the same direction as the pinned layer or in opposition to it; this is called parallel orientation and anti-parallel orientation, respectively. The insulating layer is composed of crystallized magnesium-oxide, MgO, which acts as a natural resistive barrier to the flow of electrons. When this insulating barrier is small enough, just a few nanometers, then electrons can, as defined by quantum mechanics, tunnel their way through the barrier and to the other side. The free layer changes orientation based on Spin Transfer Torque of the electrons and the direction of the current.

Parallel orientation can be generated when electrons pass through the pinned layer first, represented in *Figure 1A* below. The electrons take on a specified orientation that matches the fixed layer's magnetic orientation. Due to the electron's spin polarization they will apply a torque onto the free layer causing the free layer's magnetic orientation to match the fixed layer's. During this process some electrons will be reflected back towards the pinned layer but since the pinned layer is fixed it will have a negligible effect. To generate antiparallel orientation, *Figure 1B*, the electrons must flow from the free layer to the pinned layer. Since, the electrons are flowing in the opposite direction as the previous explanation, then the torque will be applied in the opposite direction causing some of the electrons to bounce off of the pinned layer. If enough electrons bounce off the pinned layer, where they will then take up the magnetic orientation opposite to that of the pinned layer, then the torque they exert will cause the free layer to become anti-parallel.

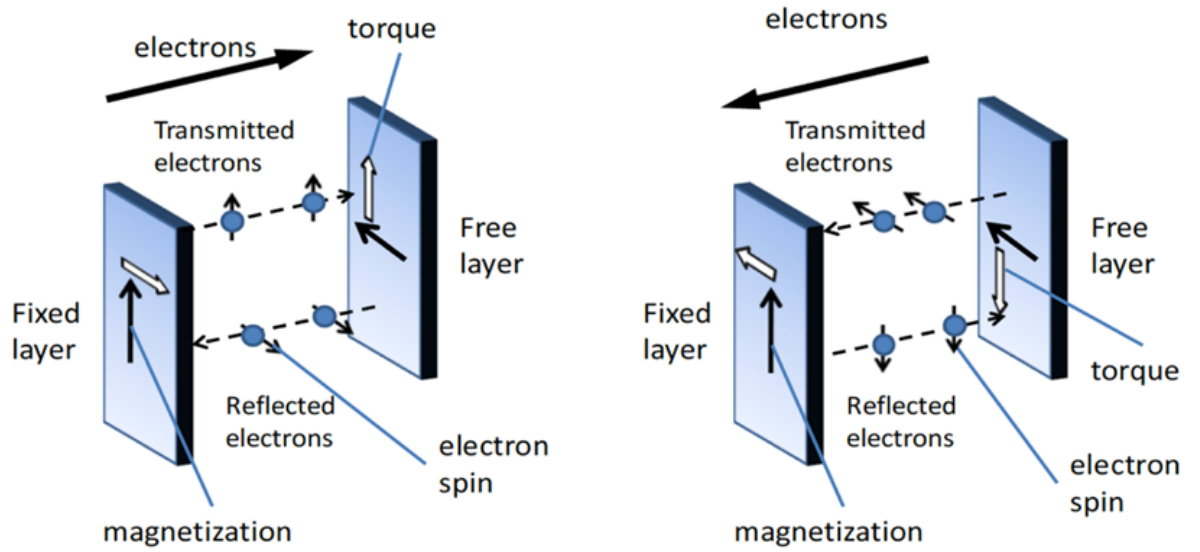

Figure 1. Physics of a MTJ from: Iong Ying Loh, Master Thesis, MIT, 2009

2.3 MTJ Operation Mechanism: Read & Write

The orientation of the free layer with respect to the pinned layer can be interpreted as a binary system. When the layers are parallel to each other, a configuration that has a low resistance, the state can be interpreted as being a zero. If the layers are antiparallel, a configuration with a high resistance, the state can be interpreted as being a one. We can use this binary Magnetic Tunnel Junction system to represent one bit of memory data or a memory cell. In order to read the bit value of the memory cell a current must be passed through the MTJ that is well below the critical write current, the current value that causes the MTJ free layer to change orientation. This low read current is used to sense the resistance of the MTJ and convert it to binary voltage u.

The process of writing data values to the MTJ is the same as changing the free layer's orientation from parallel to antiparallel or antiparallel to parallel. In order to write data to the MTJ a current must be supplied that meets or exceeds the critical write current.

3. Proposed Design: Precharge Sensing Non-Volatile Latch

3.1 Precharge NV-Latch

Precharge Latch refers to a method of sensing the resistive state of MTJ cells and converting it to a binary voltage and latching it at the output. In the Precharge Latch, as displayed in *Figure 2*, two MTJs are used as resistive memory cells to hold the data as binary one or zero. For the read mode, the input is Sense ENable (SEN). The outputs are the differential voltage outputs referenced as Q for the left side of the circuit and Q' for the right side of the circuit. For the write mode, there are four inputs: WEN1, WEN2, WEN3, and WEN4.
The three inverters that appear directly around the MTJs are the write drivers. This portion of the

circuit's job is to collect a signal from WE#, write enable input, where # ranges from one to four, and depending on the input signal determines whether write current flows from the bottom up or from top down through the MTJs. The direction of the write current will determine which of the two MTJs will be parallel and antiparallel. Essentially, WEN controls the data written to the memory cell.

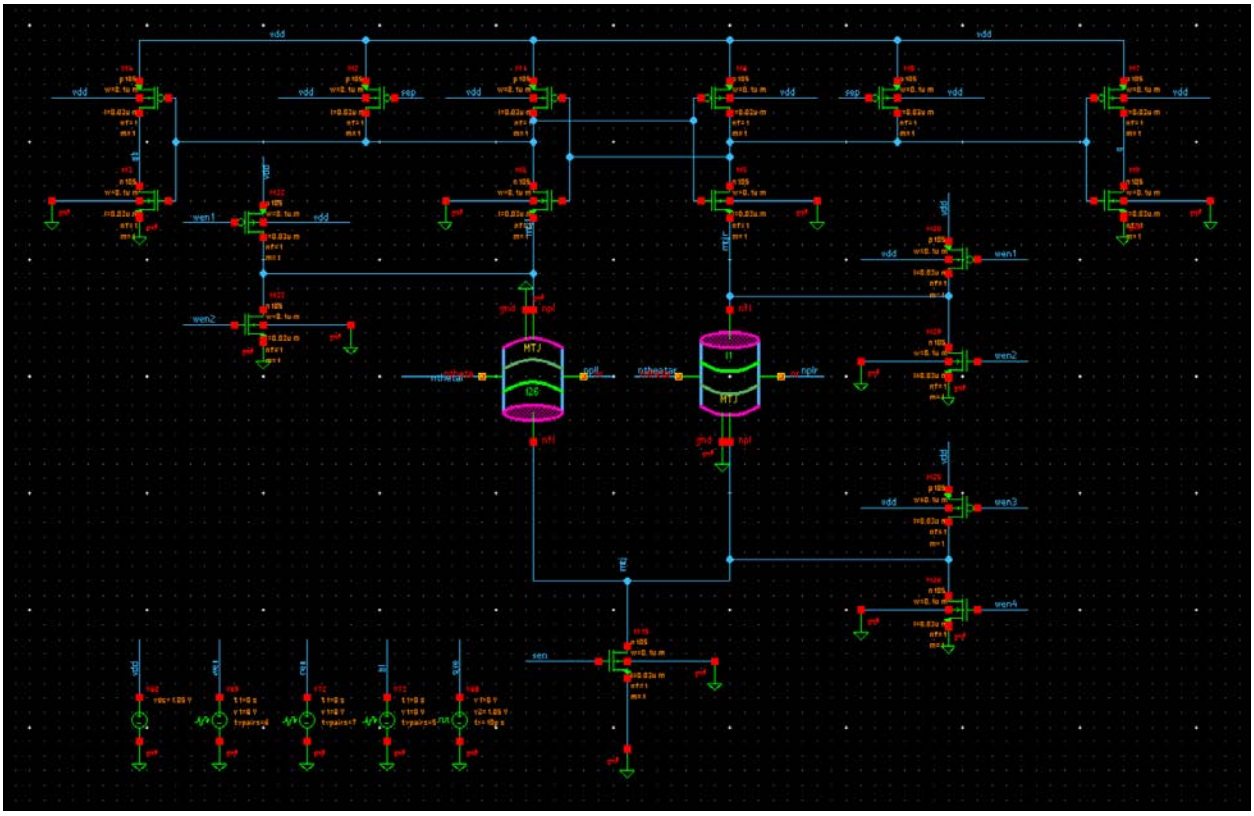

Figure 2. HSpice Circuit Diagram of Precharge NV-Latch

The bottommost transistor is the Sense Enable section, SE, while the top most section comprising of ten transistors placed to be symmetric down the middle is the Sense Amplifier. Vdd bias enter and travels down the left and right side of the Sense Amplifier and travels through the transistors until it reaches the MTJs. At the MTJs, it continues down through the MTJ with the least resistance, the one that will be in a parallel state. The two currents passing through the two MTJS and to the ground via the SE transistor will have some difference set by the differential sate of the two MTJs. This current differential is amplified by the circuit above the MTJs and produce full swing logic one or zero at the differential outputs Q and Q'.

For the write operation the four WEN signals need to be set according to the data to be written to the latch such that the correct NMOS and PMOS transistors of the write drivers are turned ON and OFF to set the current direction for proper differential programming of the two MTJs.

Moreover, these WEN signals need to set such that when the global WEN is disabled, all the write drive transistors become OFF. A decoding logic circuit can produce theses local WEN signals form the global WEN and the data input as shown in Fig. 3.

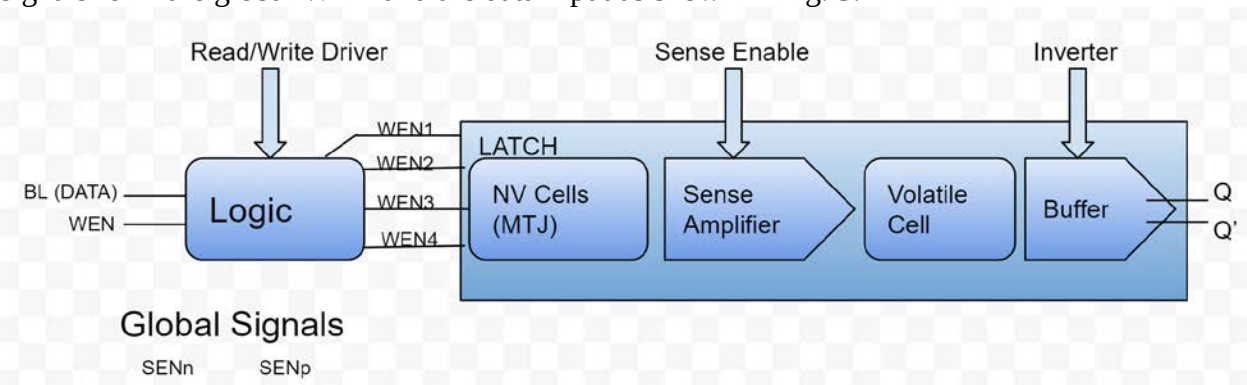

Figure 3. Block Diagram of Write Driver Logic and Precharge Latch

3.2 Write Driver Logic

The local WEN signal are controlling the gate terminal of the transistor they are connected to. A PMSOS transistor is ON when its gate is at zero and NMOS is ON when its gate is at logic 1. With this understanding and according to the desired direction for the current to flow in MTJs during the write operation, the state of the local WEN signal can be derived from the global WEN and the data to be written to the latch as shown in Figure 4. This truth table can then be converted to a logic circuit which is composed of two NAND gates and two inverters.

Bit-Line (Data)	**WEN**	WEN1	WEN2	WEN3	WEN4
0	**0**	1	0	1	0
0	**1**	1	1	0	0
1	**0**	1	0	1	0
1	**1**	0	0	1	1

Figure 4. Truth Table for Write Operation Logic

4 Optimization of Precharge Latch Write Cycle

4.1 Multivariable Simulations of Precharge Latch Write Cycle

We need to run multivariable simulations to see how varying transistor values affect write speed

and to determine much more accurate optimal width value ranges. The multivariable simulations require too much processing power and time, so we decided to simplify the write testing circuit as much as possible. First, we split the circuit into two distinct parts; the Read and the Write operation. These two operations run separately and only slightly affect each other due to capacitive effects. The write cycle optimization is done first because it is less influenced by the read circuit. The read operation is more sensitive to the sizing of the write circuit and thus is optimized last.

The multivariable simulation netlist we set up for the Write cycle has four variables. We only needed four variables to represent the six Write cycle transistors because the two Write inverters above the MTJs are symmetric. Hence, write simulations are performed with the four transistor width variables TopNmos, TopPmos, SinkNmos, and SinkPmos.

Figure 5 below shows thousands of combinations simulated to identify the relationships between the Write cycle transistors and determine the optimal width value combinations.

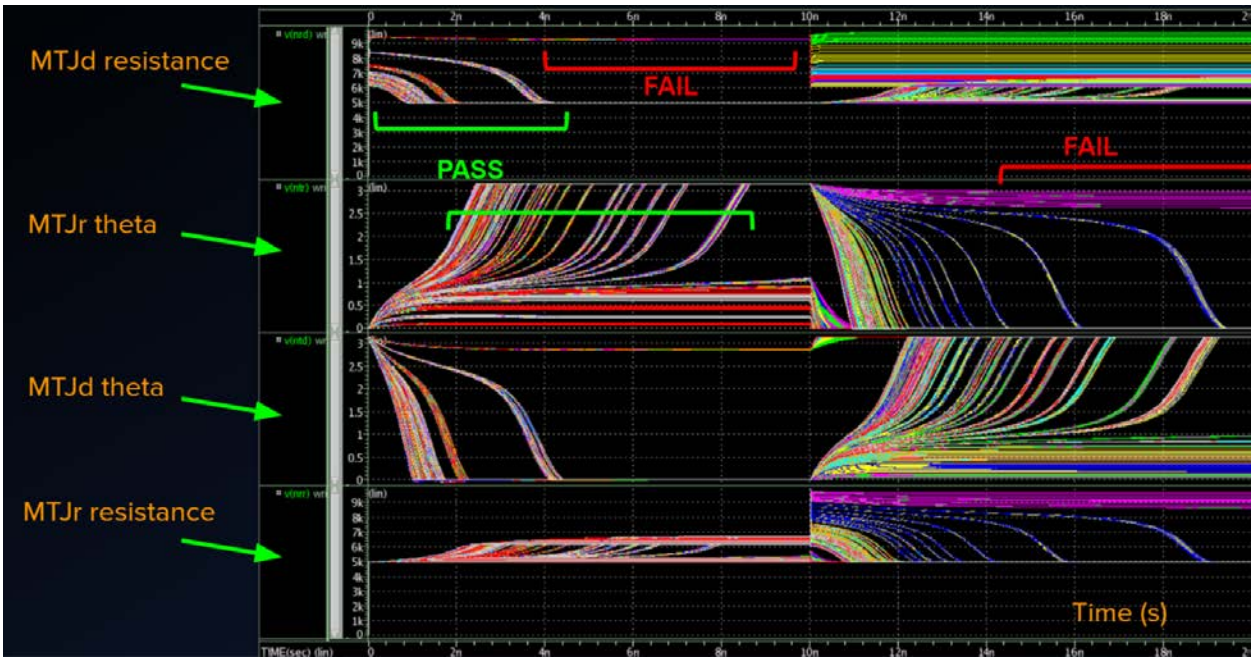

Figure 5. HSpice Graph of Write Operation Simulations, MTJ resistance and orientation

The data analysis showed that the lowest write delay is no less than 2n. This also correlated with largest area; 30+ μm. The minimum area without any write failure was 10μm and all four of the transistors had minimum values well above 0.1μ. Our data showed failures for many values and combinations; failure was determined by either of the MTJs not flipping after 15n seconds. Data analysis also showed that in most good runs, topNmos was consistently the smallest value width (under 2μ), followed by topP (around 2.5μ), sinkN (around 3μ), and sinkP (around 4μ).
Once the ranges were narrowed for each width, more sweeps were run with higher resolution.

Our next task was to find the combination of transistors that would give us the least area while still operating at less than 3n delay in the write cycle.

4.2 Monte Carlo Failure Rate Simulations

A Monte Carlo failure rate netlist program was used to test each set of values recorded in the optimization process. This Monte Carlo program is a statistical simulation that utilizes Gaussian distribution to test the process variations that arise during manufacturing.

The Monte Carlo can be set to run anywhere from 1 to 10000 iterations. Each set of our values was run at 1000 iterations in the Monte Carlo simulation to ensure reliability of the circuit to .1% accuracy. We looked for values that passed simulations with 0% failure rate, which meant at least 99.9% reliability at 1000 iteration runs. Figure 6 shows the three-dimensional plot of our results from our Monte Carlo simulations. The top left purple on the graph represents the lowest area and lowest delay but also represents the highest percentage failure rate. Our desired result, represented in red in Figure 6, had a varied level of delay and area but had a consistent success rate of one hundred percent.

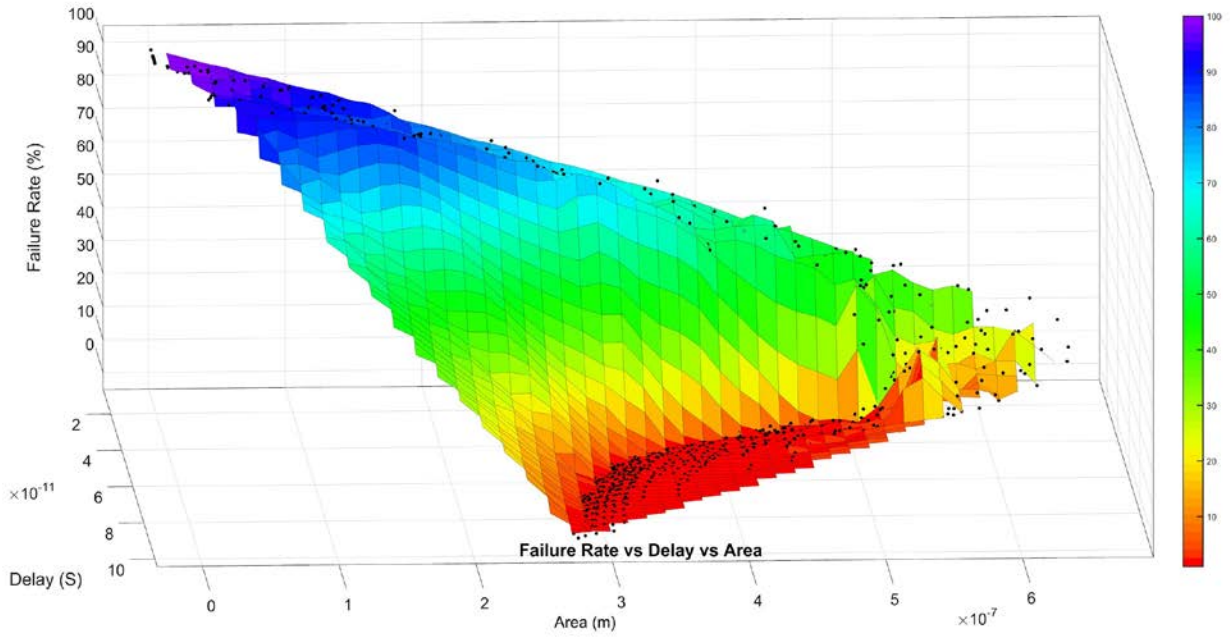

Figure 6. MATLAB Graph of Failure Rate vs Delay vs Area 3D View

5 Optimization of the Precharge Latch Read Cycle

5.1 Multivariable Simulations of Precharge Latch Read Cycle

The read cycle consisted of 11 transistors and it is necessary to optimize each of them in order to obtain the smallest possible area for the latch. The previous testing of each individual transistor

revealed that the VDD PMOS transistors in the sense amplifier did not need to be optimized and thus were left at the minimum size of 0.1 micrometers. Because of this and the symmetry of the left and right side of the sense amplifier, the total number of variables that were left to simulate dropped to four. We constructed the multivariable netlist for the Read operation simulations in the same way we constructed the Write operation netlist. We then ran a few hundred multivariable simulations and discovered that the buffer pmos transistors were also able to operate at the minimal size value of 0.1 micrometers. This fact allowed the optimization to be further simplified to three variables. In the next series of sweep simulations, we left the buffer pmos transistors, m3 and m9, at minimum size and only varied the widths of the remaining three transistors. This allowed us to increase our sweeping resolution to less than .1 micrometers. The four variables were named WN1, WN2, WP1, and WP2. WN1 represented the ground nmos m15 transistor, WN2 represented the symmetric inner latch nmos m0 and m5 transistors, WP1 represented the symmetric inner latch pmos m1 and m6 transistors, and WP2 represented the m4 and m7 output buffer transistors.

5.2 Monte Carlo Failure Rate Simulations

The Monte Carlo simulations were initially run with 100 simulations on each set of transistor values that were generated from the optimization netlist. If any of the transistor sets did not achieve 100% success, the data was recorded but the values were determined to be unusable for further simulations. The transistor values which reached 100% success were then run through the simulation again but with 1000 simulations. The majority of the transistor values failed to reach 100% success, but all of the remaining values achieved above 99.7% success rate, which meant our initial multivariable sweeps were accurate.

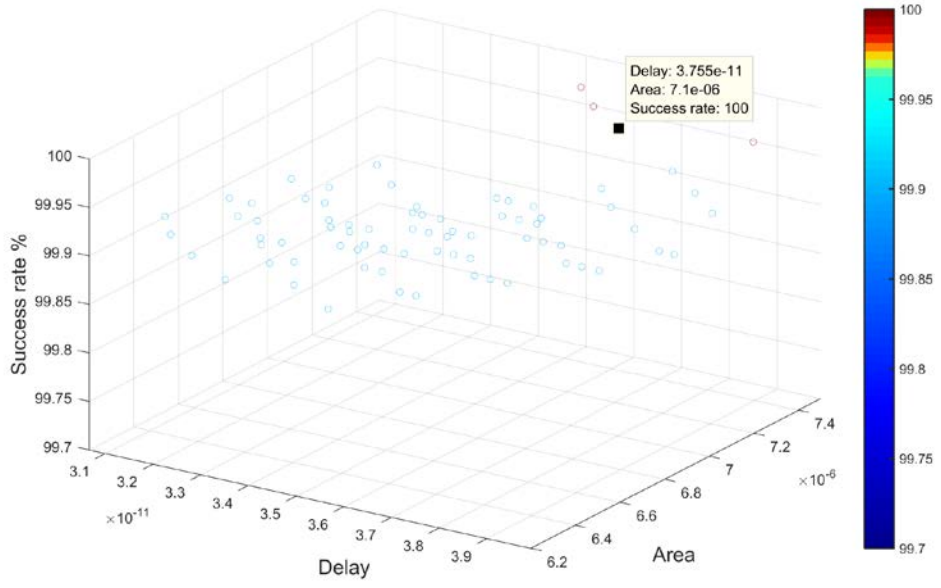

Figure 7. MATLAB Graph of Success Rate vs Delay vs Area 3D View for Read Operation

The smallest area for the 100 run was 4x0.03um2. We repeated this process for 1000 Monte Carlo and the smallest area was 7.1x0.03um2. this area passed 100% for 10000 Monte Carlo as well. The transistor widths in this set of values were 1.3 um, 1.5um, 1.5um, and 0.1 for WN1, WN2, WP1, and WP2 respectively.

6 Layout

Once all of the transistors were optimized we designed the physical layout of the circuit as shown in Figure 8. The goal of the layout was to minimize the area of the circuit. In Figure 8, *sinkn, bufferl, invl, invr,* and *bufferr* comprise the read section of the circuit while *updriverl, updriverr,* and *downdriver* are the write section of the circuit. The final constructed size of our circuit ended up being 1.672µm by 10.988µm, which resulted in a total area of 18.37um2.

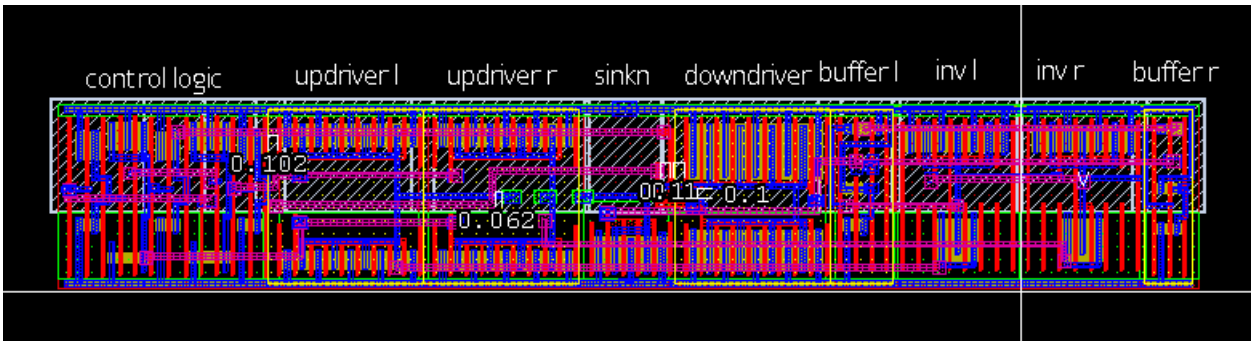

Figure 8. HSpice Full Latch Layout at Optimal Area

7 Post-Layout Results

The final test run is the Layout Parameter Extraction, LPE, which calculates the electrical parasitics present in the circuit. The parasitics are important for getting final, and most accurate, performance measurements of the circuit. With the layout complete and layout parasitics generated by the LPE, we inputted all of this data back into the hspice netlist of the full circuit to run further tests on it. We ran the write path of the full circuit with parasitics to measure our new write delay. Our real write delay was 3.5 nanoseconds. We then ran the read path of the circuit with parasitics to measure sensing delay and sensing power. Our sensing delay, measured as the time from when Sense Enable goes high to when Q and QB are updated, was 168 picoseconds. Our sensing power was 42.4 microWatts. The SE frequency at which this power was measured was 250 megahertz (MHz). The full circuit was also run in standby/idle mode, which means no input signals were generated. This was done to measure the leakage power over one cycle. The leakage power over one cycle was 1.5594 microWatts.

After the initial tests with the parasitics, we also ran a 1000 iteration monte carlo run to test the reliability of the circuit. Our results for the 1000 iteration monte carlo runs were 100% pass rates for both the Write and Read paths.

8 Student Surveys

Table 1, 2 and 3 summarize the results of pre- and post-program student surveys designed to measure perception and overall impact of the research internship program on student participants. From Table 1, it is observed that while generally students had high level of agreements to all questions asked on the purpose of doing a research internship, they noticeably showed a higher level of confidence in choosing a STEM research career after the internship. This shows that doing a research internship offers students a better insight into nature of STEM fields so that they can better decide if they want to pursue STEM research.

Table 2 shows that the participant had a high level of satisfaction with different parts of the internship program. Table 3 shows the improvements in technical skills obtained by students going through the internship program. Most notably students' understanding of a scientific approach to real problems improved significantly. Students also showed improvements in understanding the research process, integrating theory and practice, analyzing data and other information, giving an effective oral presentation, and scientific writing.

Table 1. Survey on Purpose of internship. *1 - Strongly Disagree and 5 –Strongly Agree.*

	Post	Pre	Diff
gain hands-on experience in research	4.09	4.79	-0.69
solidify my choice of major	3.56		
gain skills needed to successfully complete a BS degree	3.88		
clarify whether graduate school would be a good choice for me	3.69	4.15	-0.46
clarify whether I wanted to pursue a STEM research career	4.06	3.79	0.27
work more closely with a particular faculty member	3.75	3.58	0.17
get good letters of recommendation	3.59	4.00	-0.41
have a good intellectual challenge	4.34	4.55	-0.20
read and understand a scientific report	4.03		
write a scientific report	3.97		
ask good questions related to the scientific process	3.97		
set up a scientific experiment	3.56		
work with others to plan and conduct scientific experiments	4.09		
talk to professors about science	4.00		
think like a scientist	4.03		

Table 2. How satisfied are you with each of the following? 1 being LEAST satisfied and 5 being MOST satisfied.

Opening Day at SFSU (June 6th)	4.37
Faculty Adviser Description of Project (June 6th)	4.11
Meetings with Graduate Student Mentor	4.24
Meetings with Faculty Adviser	4.13
Mid-Program Presentations (July 21st)	4.14

Final Presentations (August 12th)	4.48
The results of your project	4.19
Your final poster	4.00
Your final presentation	4.43
How much you learned from the program	4.28
Your group mates	4.50
Your faculty adviser	4.35
The Summer Internship Program as a whole	4.13

Table 3. Please indicate your level of agreement with the following statements.
1-Strongly Agree, 5-Strongly Agree.

Prompt	**Post**	**Pre**	**Diff**
I was able to conduct the scientific research that is part of my summer internship.	4.28		
I am confident I will transfer to a four year institution .	4.78	4.64	0.14
I am confident I will complete a BS in a STEM field .	4.69	4.55	0.14
I can imagine myself continuing after my BS to pursue a Master's Degree in a STEM field .	4.38	3.85	0.53
I can imagine myself continuing after my BS to pursue a Ph.d. in a STEM field/Medical School/other education beyond the Master's level.	3.72	3.48	0.23
I have a clear career path.	4.16	3.94	0.22
I have skill in interpreting results.	4.22	4.09	0.13
I have tolerance for obstacles faced in the research process.	4.38	4.18	0.19
I am ready for more demanding research.	4.28	3.85	0.43
I understand how knowledge is constructed.	4.03	3.76	0.27
I understand the research process in my field.	3.81	3.42	0.39
I have the ability to integrate theory and practice.	4.00	3.76	0.24
I understand how scientists work on real problems.	4.13	3.70	0.43
I understand that scientific assertions require supporting evidence.	4.53	4.33	0.20
I have the ability to analyze data and other information.	4.25	4.09	0.16
I understand science.	4.28	4.12	0.16
I have learned about ethical conduct in my field.	3.84	3.97	-0.13
I have learned laboratory techniques.	3.78	3.76	0.02
I have an ability to read and understand primary literature.	4.06	4.12	-0.06
I have skill in how to give an effective oral presentation.	4.31	4.00	0.31
I have skill in science writing.	4.16	3.76	0.40
I have self-confidence.	4.22	4.27	-0.05
I understand how scientists think.	4.06	3.79	0.27
I have the ability to work independently.	4.50	4.33	0.17
I am part of a learning community.	4.34	4.33	0.01
I have a clear understanding of the career opportunities in science.	4.28	3.97	0.31

9 Conclusion

Via a summer research internship program, four undergraduate students from a community college were involved in a research program in a 4-year university in the area of non-volatile latch design using nano-scale Spin Transfer Torque Magnetic Memory (STT-MRAM) technology. The students were mentored by a graduate student and supervised by a dedicated faculty member in charge of the research project. The student interns were tasked to perform design optimizations on a non-volatile latch designed in STT-MRAM technology. The students were also required to prepare written and oral presentation on their research findings. The student interns were surveyed at the end of the program to measure their satisfaction with the offered research experience and the impact on their educational and career perspective. The survey confirmed that the participants formed a higher level of confidence in pursuing STEM careers after participating in this program.

Bibliography

[1] H. Mahmoodi, A. Attaran, T. Sheaves, “Design of a Non-Volatile Latch using Resistive Memory Technology”
[2] H. Mahmoodi, S. Srinivasan Lakshmipuram, M. Aora, Y. Asgarieh, H. Homayoun, B. Lin and D. M. Tullsen “Resisitive Computation: A Critique.” IEEE COMPUTER ARCHITECTURE LETTERS, VOL. 13 NO.2, JULY-DECEMBER 2014
[3] W. Zhao, E. Belhaire and C. Chappert “Spin-MTJ based Non-Volatile Flip-Flop.” Proceedings of the 7th IEEE International Conference on Nanotechnology August 2-5 2007, Hong Kong
[4]Wicht, Bernhard, Thomas Nirschl, and Doris Schmitt-Landsiedel. "Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier." IEEE JOURNAL OF SOLID-STATE CIRCUITS , VOL.39 NO.07, JULY 2004
[5]Welser, Jeffrey, S.A. Wolf, and Phaedon Avouris. " 282 CHAPTER 8 APPLICATIONS: NANOELECTRONICS AND NANOMAGNETICS ." Nanotechnology Research Directions for Societal Needs in 2020. London: Springer Dordrecht, 2011.