Reverse engineering as a means to understand complex tool design

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Abstract
The tools used in semiconductor processing are superb examples of advanced design for technology. They push the envelope of our process understanding and control in terms of physics, chemistry and mechanical precision and are self-contained microcosms of multi-disciplinary design. This paper describes a project to reverse engineer the design of an Anelva 1015 3-head sputtering tool. Cluster tools are now widely used in the semiconductor industry for metal and dielectric deposition. This is an early version that was donated by Intel to the Microelectronics Teaching Factory at ASU East.

A 4-stage self-paced team project activity has been developed. The first stage parameterizes the sputter process using the known operational features of the tool. The second is a set of individual activities to quantify the features of the major sub-systems. The final stages bring the team together again to analyze the trade-offs in the final system and how it has since evolved for volume production. The reverse engineering approach allows many complex design issues to be appreciated in the context of the practical realization of a commercial tool. Comparisons with current-generation tools show the continuing evolution path and new design outcomes.

Introduction

The products of microelectronics technology proliferate in our daily activities as each generation of new products delivers more computing power at lower cost. Applications that impacted a whole university budget scarcely 25 years ago are now personal desktop necessities.

Ironically, the underlying production technology that gives these great computer products is moving in the opposite direction. The reason is that digital functions can be realized with small devices and although the production tools are expensive, the value of the products they create is proportionately greater still. The trends are summarized in Figure 1.

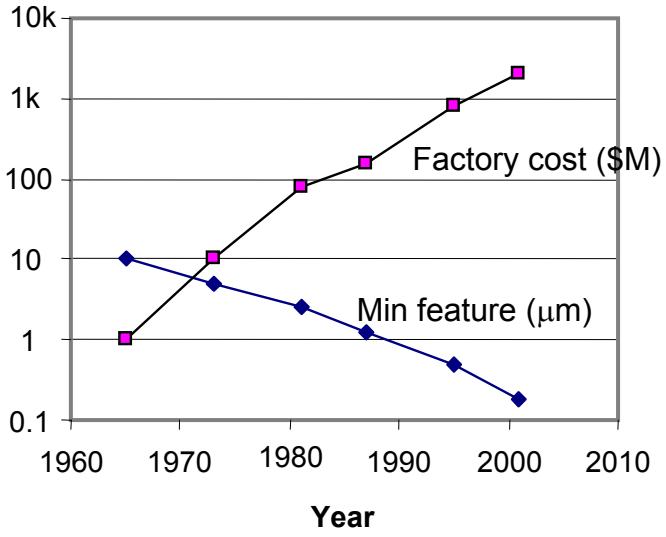

Figure 1. Transistor minimum feature size and typical factory cost

The down-side is that transistor structures that could once be made in a simple lab now require expensive tools, ultra clean conditions and operation at the limits of our understanding and control in subjects as diverse as optics, precision mechanics, ion physics and materials. Advanced semiconductor fabrication is now beyond the budget of most universities so we have to find indirect ways to deliver courses to illustrate the practical aspects of current technology.

Educational objectives

The Microelectronics program at ASU is aimed squarely at preparation of students for the workforce and the educational development of those already in the industry. Semiconductor companies in Arizona employ about 30,000 people and given rapid technology development and global business competition, the need for skill enhancement is unremitting at all levels. To further define and realize our broad educational objective, there are a number of important supporting factors:

- The Microelectronics Teaching Factory (MTF) is a 15,000 sq ft clean room that is run as a managed facility for teaching and research.
- The Industry Advisory Board is composed of operations managers from all the local companies. They view the ASU program as an investment in their own intellectual capital.
- Through two NSF grants, there are collaborations with local community colleges, schools and the Arizona Science Museum to use the MTF.
- The companies have generously donated equipment and support for the major process functions in the MTF.

Examples of curriculum development have already been reported (1) but we still face a basic dilemma. Our stakeholders expect the educational process to deliver added value in the workplace. On the other hand, it takes a long time to cover all the contributing concepts in a multi-disciplinary activity. In other words, if we take the conventional bottom-up academic approach, we never get to an applicable outcome. If we start with current practice, it is much too complex for learners.

Our solution is to start with current technology but concentrate on 'why' the implementation exists rather than 'what' is done to make it happen. We focus on the design principles behind tools, processes and products and from there, work back to the principles taught in the lower division courses. This paper describes the application of this approach to a specific sputtering tool that is used to deposit thin metal layers but it is just an instance of a more general principle.

Sputtering is a technique that is widely used in the semiconductor industry to deposit thin metal films. Thickness is usually less than 1 μm and the business priorities call for good uniformity (across a wafer that is 150 to 300 mm diameter), high throughput (ie high deposition rate), good cleanliness and low cost per wafer. In addition, it is often necessary to deposit alloys, eg, aluminum with 2% silicon and 2% copper. This is a serious technical challenge.

A simple evaporation process would deliver the most volatile material first so the resultant film would be aluminum-rich. Sputtering uses a magnetron source to generate argon ions in a low-pressure plasma. A dc bias accelerates the ions into the surface of the alloy target. The incident ion energy is high enough to knock off every atom species encountered. The chamber and electrode geometry is carefully configured to allow most of the sputtered atoms to be collected on an adjacent silicon wafer and the resulting film composition matches that of the alloy target.

To cover any unit process of this type in a class, we use15 attributes:

1. Process objective
2. Position in total process flow
3. Impact on product
4. Evolution of technology
5. *Underlying physics*
6. *Underlying chemistry*
7. *Tool design*
8. *Process operations*
9. *Safety and services*
10. *Process validation*
11. *Control and reproducibility*
12. *Models and simulation*
13. Impact on process and product development
14. Economics of the tool and its applications
15. Future technology development

The 8 italicized topics are best taught in a class/lab context.

System context

The approach taken to cover sputtering technology is illustrated in Figure 2:

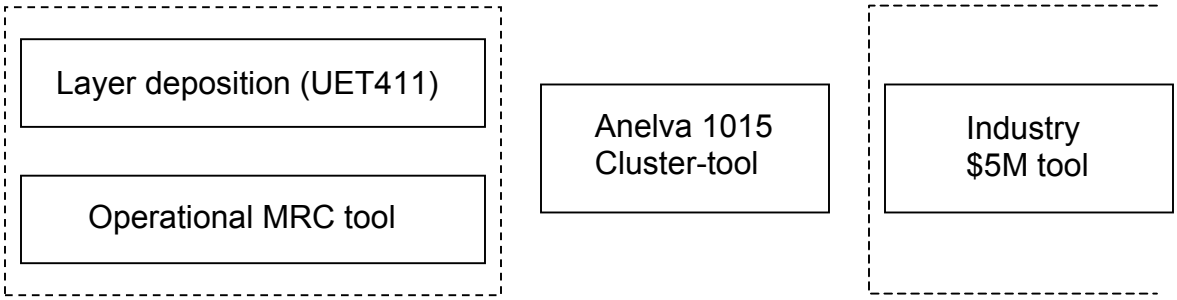

Figure 2. Anelva sputter tool as a bridge to industry practice

The operational sputter tool in the clean room was made by MRC and donated by Motorola. It is a good workhorse that meets our practical needs and modest budget. In combination with the conventional class (UET411), it provides a good introduction to the technology of sputtering. However, the industry has moved on and now operates at a much more sophisticated level. A typical tool costs about $5M and executes several functions in a cluster of workstations. The total system is much more complex than our MRC tool and we needed a way to bridge the gap. We also need a means to demonstrate principles of operation without tearing apart the working MRC tool.

Fortunately, Intel had donated an Anelva 1015 3-head sputtering tool. It is an early version of today's typical cluster tools. It is a large machine (> 2 tons and 12 m^3), and demonstrates all the major features of design and system configuration. The cost to operate such a tool is prohibitively expensive so there was little heart-searching when it was designated as a non-functional design demonstrator.

The tool features automated cassette loading and wafer handling for high throughput consistent with cleanliness and low damage risk. After the plasma cleaning station, there are 3 sputter heads with magnetron sources rated at 20 kW. They can be used with 3 identical targets for maximum throughput or alternatively, 3 different layers can be deposited sequentially without breaking vacuum.

The main features of the tool are illustrated in Figure 3.

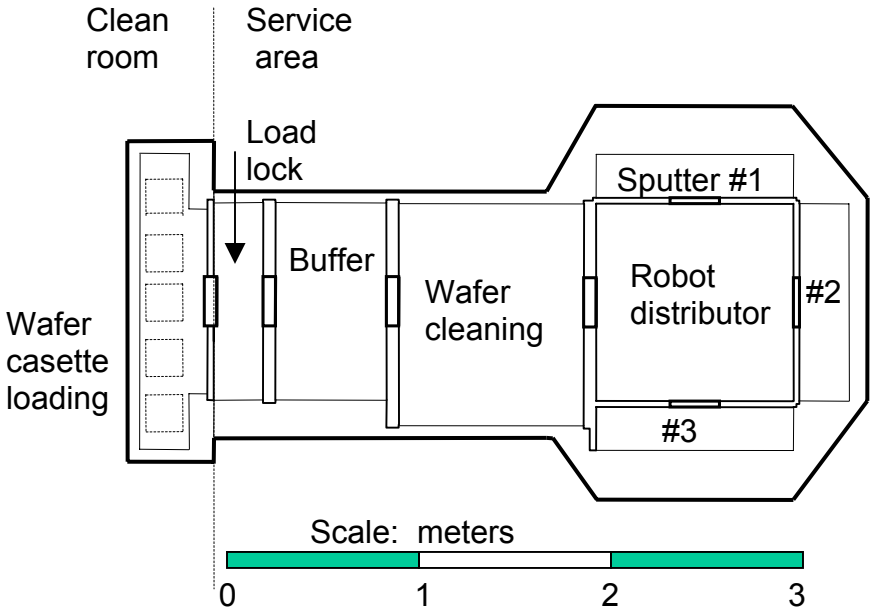

Figure 3. Plan view of Anelva 1015 sputter tool.

Each process chamber has its own cryo-pump with a shared backing vacuum line. The other main tool features are:

- 20 minute cycle time for a cassette of 25 wafers (150 mm).
- Sputter rate > 0.9 mm/minute
- Alloy composition ± 15% within wafer and wafer to wafer
- Thickness uniformity ± 5% within wafer and wafer to wafer

The reverse-engineering project

The project is designed as a self-paced lab-based activity for a team of 4 students. There are 4 phases.

1. Parameterize the sputtering conditions

The starting point is a conventional treatment of the physics of ion creation in a plasma and subsequent metal sputtering from a target as a result of argon ion bombardment. The team has the process recipe (pressures, power levels, etc) and can measure physical dimensions on the tool. The goal is to find the parameter set that gives the best description of performance and determine its sensitivity to any likely variables.

2. Individual study of sub-systems

There are 4 individual tasks to confirm the design of major sub-systems. The goal is to have the team members emulate the work that was done by the Anelva engineers when they designed the tool, ie. repeat the design process, not try to improve it.

- Vacuum systems (including chamber materials)

- Handling conditions for 150 mm wafers
- Power distribution and machine services
- Process monitoring and control

3. System assembly
The group reconvenes as a team to address how the sub-systems are combined. This is the stage where they learn that a whole system is greater than the sum of its parts. They have the final result in the form of the physical tool but no information about the engineering decision path that led to the conclusion. There are 6 topics to address:

- Configuration of the sub-systems to optimize footprint
- Safety
- Throughput
- Maintenance
- Wafer cleanliness and yield.
- Economics and operational efficiency

The goal is not to design another system; it is to deduce the steps and priorities in the design process and the obvious trade-offs that had to be made. Since the original design activity by Anelva required more than 50 person-years, ours is a highly simplified and accelerated process.

4. Bridge to current practice
Extend the Anelva experience to review current tools and their development in the context of the International Technology Roadmap for Semiconductors (2).

Conclusions and future development
Reverse engineering of an established product is a very effective learning platform that illustrates many principles within the context of a viable application. In principle, it can be applied to any engineering product but there are several additional factors that make the approach very useful for microelectronics. The most significant is that no semiconductor fabrication tools are produced in large numbers – a few hundred at most – before new technology developments force radical change. As a result, we don't have to search through the vast number of incremental improvements that usually characterize volume production tools. The design decisions and the progression by which they were reached are logical and can be uncovered with modest effort.

The project has so far been run in 2 trial phases. The whole sequence has been run by Brian Wales, one of the authors, as a single student project. The system integration factors that link safety, throughput and maintenance have also been analyzed as a series of team activities. The final stage will integrate these activities into a self-paced lab program. As well as ASU students, it will be available (with appropriate modifications) to our community college partners. A similar activity is being developed to demonstrate wafer stepper design for high quality optical lithography.

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Bibliography

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2. The International Technology Roadmap for Semiconductors (ITRS) is fully described in an extensive web site at http://public.itrs.net.

Biographical information

John Robertson is a professor in the Department of Electronic and Computer Technology at ASU's East campus in Mesa, Arizona. From 1994 to 2001, he was Director in Motorola's Semiconductor Products Sector and before that, Professor of Microelectronics in Edinburgh University, UK.

Brian Wales is a pre-silicon design engineer for Intel Corp – Consumer Electronics Group in Chandler Arizona. He is also currently a Graduate Student at Arizona State University. From 1996 through1998, he worked at Intel's Fab-6 facility where he ran day-to-day operations with the Anelva 1015.

Jon Weihmeir is currently a visiting professor at ASU's east campus from Motorola's Semiconductor Products Sector. From 1996 through 2002, he held management positions in process engineering, device engineering, and manufacturing at several production facilities in Mesa, Arizona