Schematic Capture as an Entry Program for Electronics Analysis

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Abstract

Schematic capture software programs provide a convenient and meaningful way for students to interface with other electronics analysis software programs. In the early analog and digital electronics courses the student becomes quite familiar with the associated hardware components, but entry into the various software programs remains a mystery. The difficulty in using computer analysis programs is that students are required to use an unfamiliar language. Because of the time involved in learning this new software language, the computer analysis of electronics circuits is sometimes delayed to a later course.

CapFast[1] is a flexible and useful circuit design software tool for electronic design engineers. The CapFast software has many functions and features that make students productive sooner. They can draw the circuit schematic with standard component symbols using drop and drag techniques. This makes it easy for them to draw and modify the circuit schematic. Including CapFast software as an integral part of a course allows more time to teach the theory because computer simulations can be used with a common schematic entry point.

This paper explains the actual program functions that allow CapFast to be used as a schematic entry to interface with PSpice[2], for an analog circuit, and with CUPL[3] for a digital circuit to be programmed in a PLD. Students use the software as a prelab exercise. Then the actual electronics laboratory was conducted to verify the simulation tool. The students were pleased with the experiments because they could do computer simulation using the schematic as the entry point. Using a schematic as the entry point for electronics computer simulation programs is an advantage over writing the netlist files by hand. CapFast is a schematic capture program which interfaces with a variety of electronic design software programs.

Introduction

CapFast software creates files that maybe used by many electronics analysis software packages to analyze the operation of the original circuit. This schematic entry is very useful when circuit conditions change, such as changes in the component values, input signal levels, and voltages. The simulation files created by CapFast are used in PSpice, CUPL and Susie[4]. The addition of CapFast software to a course makes it easier for the student because they learn only one schematic entry program. This program provides the netlist for other software programs. CapFast also reduces the mistakes that students make when they are required to enter netlist files for the various software packages.

CapFast Schematic To PSpice

The first example is to plot the voltage across the resistor and the voltage across the inductor as the frequency of the input voltage is varied from 100 Hz to 10 KHz. A second plot is made of the time domain voltage across the resistor, the voltage across the inductor, and the current through the resistor. These values are to be plotted for the input voltage shown on the schematic. The circuit shown in Figure 1. is used for the analysis.

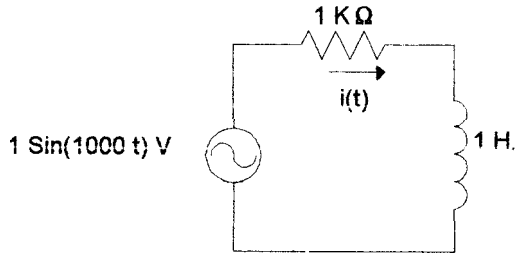

Figure 1. Circuit for entry in PSpice.

All of the output plots required can be created using PSpice. Therefore, this example will use CapFast to create the PSpice netlist.

Using CapView to draw the circuit

The creation of the circuit diagram in CapFast is made by selecting the Schematic Capture icon from the main menu. The drafting process is similar to schematics created with other drafting programs. Components needed to draw the circuit are found under the Get Parts menu listing. Since the analysis is to be completed using PSpice, the parts are selected under the Spice Library submenu. The parts are placed on the drawing area using the familiar drop and drag placement method. This method is illustrated below. The purpose of including these steps is so that one can see the actual programming procedure. These steps indicate the ease in which programming is accomplished.

To insert an inductor on the drawing requires the following keystrokes. Press (g) for Get Parts, then press (s) for Spice Library, press (p) for Passive Components, and press (i) for Inductor. The symbol is now (in green) on the screen. Use the mouse to position the inductor and press the left mouse button. The properties list for the inductor will appear on the screen, move the cursor over the word (value) in the line that says (-DN value:) to make the (-DN) turn red. Then press (v) for value. At the bottom of the screen there will be a line that reads: Please enter new value value:, type(1) for 1 Henry. Press (d) for Display and the 1 will turn yellow. Press (m) for Move, a 1 now appears on the screen, use the mouse to position the 1 near the inductor and click the left mouse button, press (Esc) to exit.

To rotate the inductor to a vertical position requires the following menu keystrokes. Press (e) for Edit, (2) for 270 Degrees. The Inductor will rotate 270 degrees. After the inductor has been rotated it may have to be moved to the proper location. To rotate the value to make it easier to read requires the following keystrokes. Press (p) for Properties, move the cursor over the word (value) in the lime that reads (-DN value: 1) to make the -DN turn red. Then press (o) for orientation, and (u) for up, (Enter) to change the orientation.

When all of the components have been placed, connecting lines must be drawn. As each line is drawn, the software automatically asks for a wire number. The most convienent numbers would be the PSpice node numbers. In the second example there is no reason to number the wires. The next step is to label the components so that they can be translated into PSpice.

Label the components

Labeling components is an important step that must be done in order to create the PSpice netlist. Labeling the resistor, R1, requires that text be added to the drawing. The following keystrokes will place text on the schematic. Press (t) for Text, Press (r) for Relabel. Type (RI) which will be displayed at the bottom of the screen. Press (Enter) to Move, then click the left mouse button when the text is properly placed.

After all components have been properly placed and labeled, it is necessary to add a TRAN statement because of the voltage plot specification, and an AC Analysis statement because of the required frequency plot. These parameters are required because the circuit is to be analyzed using PSpice.

The TRAN parameter is found under Get Parts, Spice Library, Meters/Controls menu selections. The required values to be added are labeled with *req* in the properties list. The TRAN statement requires values for the stop time (tstop) and the time step (tstep). For this example .2m and .02m were selected in order to display two complete cycles.

The AC Analysis is found under the Get Parts, Spice Library, Meters/Controls menu selections. The parameters that must be entered are Fstart, Fstop, and ND(number of steps). The initial problem specifications are used for these values, Fstart= 100, Fstop= 10K, Nd=25. The labeled schematic as drawn in CapView is shown in Fig. 2.

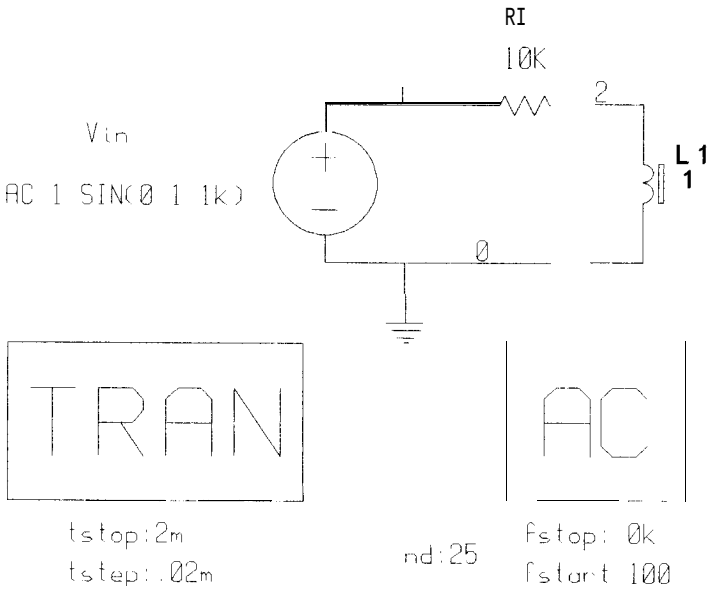

Figure 2. Example 1. as Drawn in CapView,

Save the completed schematic

The work just completed is saved under the File, Write menus. When the file was saved it was named EXP 1. CapFast automatically adds a . SCH extension to the program name. Then press (f) for File and (q) for Quit, to exit the CapView program.

Create the PSpice .CIR file

To create the PSpice netlist file, select the Simulator Interface icon from the main menu then select the Sch to PSpice icon. The next screen requires that the filename be added to sch2spi -QPSPICE. (In this case: sch2spi -QPSPICE EXP1). CapFast then creates a file named EXP1.CIR. This is the PSpice netlist file and is shown in Figure 3.

```
CIRCUIT: EXP1 DATE: MON NOV 2710:08:441995
L120 1
R1 12 10K
VIN 1 0
+ AC 1 SIN(0 1 1K)
.AC DEC 25100 10K
.TRAN .02M 2M
.END
```

Figure 3. PSpice netlist for Example 1,

This file can be read directly into PSpice where the analysis can be performed.

CapFast Schematic To a CUPL PLD Programming File

The second problem is to program a GAL 16V85 chip to function the same as the circuit shown in Fig. 4. The PLD chip is to be programmed so that A is on Pin 1, Bison pin 2, the NAND output is on pin 12, and the XOR output is on pin 13.

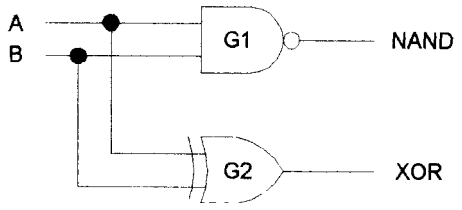

Figure 4. Schematic for Example 2.

Drawing the schematic using CapFast

The only difference between the creation of this schematic to the one created in Example 1 is that the parts are selected from the Symbol library under the Get Parts menu instead of the Spice Library. Parts must be named by typing in the part name before they can be placed. Permissible part names are: INVR, ANDx,

NANDx, ORX, NORX, XOR, XNOR, where x is the number of inputs. Logic devices must be labeled Gx, where x is a unique number. Input and output edge connectors must be labeled. The input connector is identified MO, the output connector as M2. In the properties list the reference pins (ref:PINx where x=PLD pin number) must be labeled. The labeled schematic for Example 2. is shown in Fig. 5.

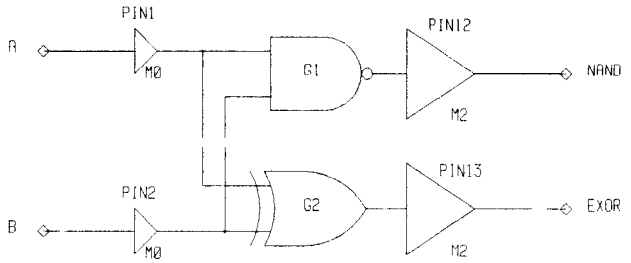

Figure 5. CapView schematic for Example 2.

From the CapFast schematic to CUPL

The schematic drawing is completed and then saved as EXP2.SCH. The CapFast file SCH2PCB, is executed by typing SCH2PCB EXP2. SCH from the command line. The execution of this SCH file creates a PCB netlist file called EXP2.ASC. In CUPL this .ASC file can be executed under ONCUPL, part of the CUPL program, to create a .PLD file. Instead of showing the .ASC file generated in CapFast, the more familiar .PLD file is shown in Figure 6. This .PLD file is executed under CUPL where the .JED file is created. The resulting .JED file can be used to program the G16V8. The students use either a Chipmaster 3000 or a Logic Lab programmer to program the GAL16V8.

```
Name     Exp2;
PARTNO   XXXXX;
REVISION XXXXX;
DATE     Xxxxx;
DESIGNER Xxxxx;
COMPANY  XXXXX;
ASSEMBLY XXXXX;
LOCATION Xxxxx;
DEVICE   G16V8;

/*****************************/
/**     Input pins          **/
/****  *************************/

Pin    1      = A;
Pin    2      = B;

/*****************************/
/**     Output pins         **/
/****  *************************/

Pin    12     = NAND;
Pin    13     = EXOR;
```

```
J*****************************/
/**      Pinnodes          **/
/*****************************f

/*****************************/
/**      intermediate variables**/
J*****************************/

G2      = A $ B;
!G1     = A & B;

/*****************************/
/**      output equations        **/
/*****************************/

NAND = G1;
EXOR = G2;
```

Figure 6. EXP2.PLD file that will run in CUPL.

Conclusion

The schematic entry format underCapFast isthesamelevelof difficulty as other schematic entry packages on the market .Theadvantageof using CapFastisthat schematicentrycan be learned once. CapFast can interface to various software packages. Students have used CapFast to interface with PSpice, CUPL, and Susie. CapFast software is compatable with DosandWindows platformsonthePC and on a number of engineering workstation platforms. CapFast isavailable asastudent version for $80. The site license for the IUPUI Engineering Technology network is $500.

The students have been successful in using CapFast to create the schematic as an entry point for various software packages. For large problems, the students are given a similar CapFast file on the network. The problem is then for students to make minor circuit modifications and analyze the results.

References

1. Phase Three Logic, Inc, 19545 NW Von Neumann Dr., Suite 230, Beaverton, OR 97006, (503)53 1-2410.

2. MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718, (800) 245-3022, For a flee evaluation copy of PSpice send a request on an educational letter to: Product Marketing Department, Microsim Corporation 20 Fairbanks, Irvine, CA 92718. Duplication of the disks for your students is encouraged.

3. Logical Devices, Inc., 1201 NW 65th Place, Fort Lauderdale, FL 33309, (800)33 1-7766.

4. Automated Logic Design Co. Inc., 3525 Old Conejo Rd.# 111, Newbury Park, CA 91320, (805) 499-6867,

5. Lattice Semiconductor Corporation, 5555 NE Moore Ct, Hillsboro, OR 97124, (800) FASTGAL.

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