Session 3548

Should We Teach Chip Design in Electronics Engineering Technology Programs?

A Senior Project Course in ASIC Design

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1. Introduction

Teaching circuit design up to chip layout seemed exotic for Electronics Engineering Technology(EET) programs for many years in the recent past. Many educators believed that courses like VLSI Design or ASIC Design should be destined only for Electrical Engineering students. And so did the faculty at Oregon Institute of Technology until, in the early nineties, different trends in local industry filtered back through the alumni, made us take a break-off from the old paradigm. The Computer Engineering Technology Department on the OIT campus in Klamath Falls, started offering selected courses in VLSI design starting in 1992.

Oregon Institute of Technology is a four year technology college granting bachelor degrees in different technology fields, such as electronics and computer technology. The principal campus is situated in Klamath Falls, southern Oregon.

OIT has also a presence in Portland at two different metropolitan locations offering upper division night classes for students employed in local industry. In 1993/94, the EET department started to offer the ASIC Design Senior Project Course only at the Portland campus. The sequence of EET courses in the Electronics Engineering Technology curriculum is presented in Table 1.

Year	Term	EET Course	Credits
Freshman	Fall	Introduction to Electronics and Lab	4
	Winter	Circuit Analysis I and Lab	7
	Spring	Circuit Analysis II and Lab	7
Sophomore	Fall	Semiconductor Devices and Lab	7
	Winter	Analog Devices and Circuits and Lab Introduction to Digital Concepts and Lab	6 4
	Spring	Operational Amplifiers and Lab Digital Logic and Lab	6 6
Junior	Fall	Digital Systems and Lab Network Analysis and Lab C Programming	5 4 4
	Winter	Introduction to Microcontrollers and Lab Linear System Analysis and Lab Advanced C Programming	5 6 4
	Spring	Microprocessor Systems and Lab Communication Systems and Lab	6 5
Senior	Fall	Analysis and Design of Analog Integrated Circuits/Lab Senior Project I (Intro. to ASIC Design)	6 3
	Winter	Electronics Elective Senior Project II (ASIC Design)	3 3
	Spring	Electronics Elective Senior Project III(ASIC Design)	3 3

Table 1. EET Sequence of Courses at OIT.

The senior project course is a three term sequence. Two alternative options are available for OIT students in Electronics Engineering Technology, as presented in Fig.1:

a) the individual study option where the students can choose their own subject of interest, design and implement the product of their choice or suggested by industry.

b) the structured Senior Project courses where students are guided in a particular field of electronics. In Klamath Falls EET students can take: Digital Signal Processing(DSP), RF Communication(RF) and Automated Test Engineering(ATE).

At the OIT Metro Campus in Portland, the small number of students enrolled in the senior project did not justify the offering of many different options. For years, only the individual study project was offered. The majority of students did well, but we always had a number of students who did not know what their interest was and where to start. They needed more guidance. If we could find something of broad interest for students to take as an alternative to the individual study course, we could restrict the individual study option to only really worthwhile and interesting projects . This is how we started the ASIC Design class.

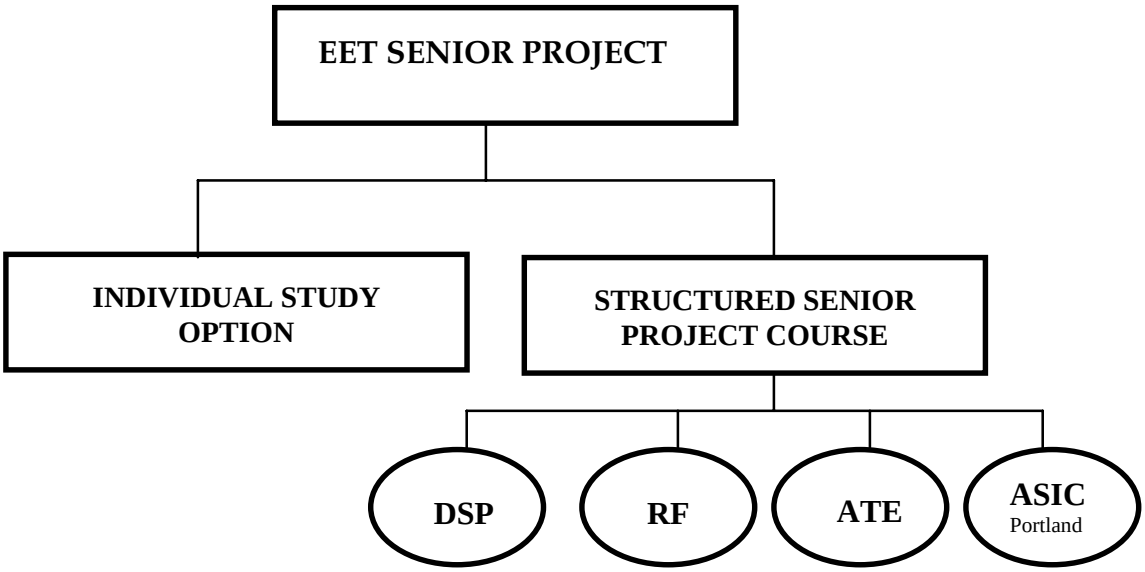

Fig.1 EET Senior Project Options

2. Content of the ASIC Course

The sequence of the ASIC course is presented in Table 1:

Fall Term	Introduction to ASIC Design	2 credits lecture 1 credit laboratory
Winter Term	ASIC Design	1 credit lecture 2 credits laboratory
Spring Term	ASIC Design Project	3 credits laboratory

Table 2 - Sequence for ASIC Design Courses

a. First term : Introduction to ASIC Design

The principal objectives of the first term course (Introduction in ASIC Design), are as follows:
a. To give students a clear understanding of what they are going to design and how.
b. To give students an overall perspective of the field of chip design, industry status and trends.

Two textbooks are recommended for use in this course:
1. John Uyemura - *Physical Design of CMOS Integrated Circuits*, PWS 1995, and
2. John Huber, Mark Rosnek - *Successful ASIC Design the First Time Through* ,Van Nostrand Reinhold 1991.

The course outline is presented below, :

1.	**Introduction to Physical Layout of CMOS Integrated Circuits** CMOS Fabrication, Layout of CMOS Integrated Circuits, CMOS Logic Circuits, Models for simulation.	12 hours [Textbook 1]
2.	**Introduction ASIC Design** Types of ASICs, ASIC Technologies, Market Statistics and Trends	3 hours [Textbook 2]
3.	**The ASIC Design Process**	3 hours [Textbook 2]
4.	**Design Implementation Phase for ASICs**	3 hours [Textbook 2]
5.	**Logic Simulation of a Design.**	3 hours [Textbook 2]
6.	**Concepts in Chip Layout**	3 hours [Textbook 2]
7.	**Advanced Topics in Logic Design** Timing in Digital Circuit, Design Fault Simulation, Embedded Testability.	3 hours [Textbook 2]
8.	**Analog ASIC Design.** Analog Simulators. Device Models. Trends in Analog EDA	3 hours [Textbook 2]

The first topic of the outline and Uyemura's book were introduced for the first time in Fall of 1996, after the instructors noticed that half way through the course, the students learned a lot about system design, but the physical aspect was lost from sight. Now they use a simple, PC based graphical editor, L-EDIT, to design simple layouts for different logical gates.

The second textbook is used only as a reference, being somewhat outdated and out of print. It still covers succinctly all issues in EDA design. Lots of overheads and slides developed over time or borrowed from faculty development workshops are used.

The laboratory activities the for this first term course are as follows:
1. Physical Design of gates using L-EDIT.
2. Demonstration Session with Mentor Graphics tool set: Schematic Capture, Digital Simulation and Synthesis.

Also, in this course, the students were required to develop a proposal for their senior senior-year project.

b. Second Term: ASIC Design - Senior Project II

In the second term course (Senior Project II), the students are supposed to learn how to design using the Mentor Graphics tool set, how to prototype the project using a programmable logic device (XILINX) and submit the final proposal for design..

During the first few years that the course was offered, we identified three areas for improvement of students' productivity in the laboratory: documentation, examples of designs, and the demo design. The following list describes the materials that we developed to address these needs:

- Designing Circuits using Mentor Graphics Tools (process-based book)
- Mentor Graphics Quick Reference Card
- Examples in common location on network
- Lecture Slides
- Completed DEMO Design

The students enter this course with their preliminary project proposals completed. At the end of the term, they should have a finalized project proposal (including block diagrams) and two design examples (BCD counter and mini-project) that they took through the top-down design process (using both schematic- and VHDL-based approaches). By the end of the term, they should also have introductory knowledge of Mentor Graphics tools and VHDL.

The second term course outline is as follows:

1. Introduction to the Mentor Tool Set

2. Capturing designs using Design Architect

3. Simulating designs using QuickSim II

4: Downloading designs onto a XILINX chip

5. Mini-project (schematic-based)
The mini-project is a 30 gate hierarchical design that allows the students to create a schematic-based top-down design. This design basically re-enforces the topics covered during the first half of the term.

6. Capturing designs using VHDL

7. Simulating VHDL designs using Quicksim II

8. Synthesizing VHDL designs using AutoLogic

9. Mini-project (VHDL based)

10. Automated IC layout using IC station

c. Third Term: ASIC Design - Senior Project III

For the third term course (ASIC Design - Senior Project III), no structured instruction is provided. Depending on student interest, miscellaneous subjects are presented such as ASIC library development, more VHDL information, advanced simulation. The students mainly work on their projects and final senior projects reports. All projects are presented as final products, consisting of a system (not just simulation waveforms or blinking lights). Presentations usually last about 45 minutes.

Some examples of project titles are: Controller for Ultra fine Wire Transport System, Bar Code Reader, Distributorless Ignition, Pinewood Derby Timer and Placer, The Stepper Motor Controller.

3. Instructional Results and Improvements in the Course.

Offered for the first time in a four year technology EET program, the course has been evaluated as a success by the students and instructors alike. The positive outcomes of the course could be listed as follows:

- All senior project students were exposed to the ASIC design process.
- The course took the mystery out of VLSI design and gave students confidence when interviewing for a IC design position.
- Students were exposed to more sophisticated EDA commercial tools at the industry level.
- A good partnership between Mentor Graphics and OIT was initiated.

The course was taught for the fourth time the 1996-1997 academic year. It evolved to the present format with the following instructional improvements introduced :

- Make students understand how EDA vendor, ASIC vendor, and the designer interact
- Use XILINX chips to prototype projects and don't go direct to silicon layout.
- Use the tools every week
- Pick only one design approach (top-down or IC layout)
- Use a DEMO design showing the entire design process from VHDL code to IC layout
- Don't start the project until one learns the tools

Give extra credit if a student implements the layout in silicon.

Some special issues have to be considered when presenting EDA tools :

- Separate "Designing" from "Learning Tools"
- Explain the handling of different levels of abstraction (components and models)
- Present "how" a tool works

Other useful practices for the success of projects are:

- Deciding when to upgrade next software version .
- Keep copies of ASIC design kit documentation in lab.
- Enforce project management

When teaching VHDL, some good practices are:

- Teach VHDL as a Hardware Description Language and not as a programming language.
- Teach that "VHDL synthesis is all about style"
- Give many of VHDL examples (emphasizing synthesis style)
- Document process of "spec" to "VHDL code"

4. Equipment and Cost of the Program

One of the biggest caveats of offering an ASIC course is the large cost of the equipment and maintenance of the laboratory. OIT laboratory has seven SUN stations (two SPARC 10 and five SPARC 2) and seven Tektronix X-windows terminals. Plotters and printers are also shared in the lab. The initial equipment investment approached for the first two years was $60,000. Mentor Graphic Corp. and XILINX donated the software.

Every year there are two maintenance contracts maintained: one with SUN Systems and one with Mentor Graphics. Cost: $4,200. Also, a system administrator is needed. OIT contracts this work outside, paying hourly wages.

The dilemma which we need to consider soon is weather we should we maintain an expensive UNIX laboratory or, with the development of PC based EDA tools, or we should transfer all training on Pentium computers with Windows NT? We will certainly consider the industry trend.

5. Conclusion

The development and offering of the ASIC class at OIT was a very positive experience for both students and faculty. The students graduated with the conviction they got an up-to-date education in design. Many of them got promoted in their organization to a design positions or got hired as designers in other companies. Some people from industry, not seeking a degree, were also enrolled in the class. Courses like this are offered by local universities as well, but apparently, the practical, "no frill" approach of the engineering technology course is appealing to

engineers. Surveys of the EET graduates showed that many consider this course one of the best training they got in the program.

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