2006-1904: SYSTEM DESIGN, DEVELOPMENT, TRAINING AND IMPLEMENTATION OF A MIXED SIGNAL BROADBAND CHIP-TO-CHIP DIGITAL COMMUNICATION SYSTEM

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Abstract

At Prairie View A & M University, we developed a new Mixed Signal Systems and Broadband Access Technology Laboratories over the last few years. These laboratories are used in helping our premier Semiconductor and Telecommunication companies in their various areas of research needs, such as, mixed signal design, testing and in interoperability and reliability studies. These laboratories are used also for the training of our students in these emerging areas of technology and for research, especially, the Digital Subscriber Line (DSL) broadband mixed signal technology.

As the paper will demonstrate, we introduce our students to the modeling and simulation of an 8-Pulse Amplitude Modulation (PAM) transceiver that can be fabricated using the Complimentary Metal Oxide Semiconductor (CMOS) transceiver technology. The transmitter incorporates a pattern generator and a pseudorandom bit sequence (PRBS) generator, which are multiplexed to a 3-bit digital-to-analog converter (DAC) with pre-emphasis. The receiver integrates three 3-bit analog-to-digital converters (ADCs) for over sampling of the transmitted data. The modeling and simulation design was implemented using Matlab/ Simulink platform.

This modeling and simulation design is developed and implemented using an 8-PAM system, which partitions the data from the transmitter into 3-bit, 8-level quantized form. This type of multi-signaling reduces the symbol rate and thus limits data error in the receiver. To boost the efficiency and reliability of the system, three ADCs are used, instead of one, sampling three times the channel data rate. In this design, a special data select code is written with Matlab/Simulink platform to recover the transmitted data. The data from the transmitter is recovered by error correction technique using the Matlab code.

As part of our goal in the Electrical Engineering and Engineering Technology Departments to expose our students to hands-on training, the students are given the opportunity to model, simulate and implement the software system design in the broadband (high-speed) communication and mixed signal systems laboratories. The results of these implementations have been encouraging. The lessons learned, future work and recommendations are discussed in this paper.

1. Introduction

The issue of low power, high-speed transceiver, chip-to-chip mixed signal communication system is one of those emerging technologies of the 21st century. It is also one of the major
challenges in present day communication systems. Researchers such as Foley and Flynn,[1, 2], have made efforts to look at this issue. Currently, optical interconnect, low voltage differential signaling (LVDS), standard bus such as Universal Serial Bus (USB) are all methods of an innovative form of digital communication from chip-to-chip. In digital communication, one form of transmission uses basis functions to associate modulation of vector spaces. The geometric representation of all the points in the vector space is called constellation, which is all possible data symbols. For instance, N-level pulse amplitude modulation (N-PAM) is an example of a constellation where the data symbols are carried by a fixed pulse shape. N-different amplitudes represent log (N) bits of data.

The channel spectral efficiency is determined by the bandwidth of the basis waveform and is measured in bit per second per hertz (bps/Hz). For example, for N-PAM communication systems, the spectral efficiency is $2 \times \log(N)$, [3]. Hence, spectral efficiency increases logarithmically with number of PAM level, N. In addition, transmitting a sequence of pulse waveforms results in data eye diagram, where the larger the eye the better the noise immunity and hence, the better the spectral efficiency.

The 8-PAM CMOS transceiver is used in high-speed serial transmission between two integrated circuits. This reduces the number of Integrated Circuit (IC) pins and printed circuit board (PCB) tracks. The 8-PAM layout design scheme reduces the channel symbol rate one-third than that of a 2-PAM transceiver for a given transfer rate [1]. The transmitter side of the transceiver contains a 3-bit pre-emphasis digital-to-analog converter (DAC). The DAC is implemented without an increase in digital computations. The receiver uses three differential 3-bit ADC’s for oversampling. From the three output samples, the recovered data is chosen from the sample that is determined to be the data closest to the data eye. The transceiver also contains a 3-bit fixed pattern generator, a $2^{10}-1$ pseudorandom bit sequence (PRBS) generator, and a verifier for built-in self-test (BIST). The delay-locked loop (DLL)-based clock synthesizer is incorporated into the transceiver design to run at three times the reference frequency for the three receiving ADCs. The DLL also actives the transmitter and is self-correcting.

As part of our goals, we want to expose our students to hands-on training and therefore give the students the opportunity to model, simulate and implement the software system design which can lead to system verifications of the chip-to-chip communication system.

2. Objectives

The objectives of this phase of the research project are to:

- Team with several instructors in integrating this experimental project and lessons learned into engineering curriculum.
- Demonstrate this experimental project and evaluate its effectiveness as an innovative engineering design for students.
- In collaboration with industrial partners, evaluate and explore the possibility of commercialization upon demonstrated success.
- Work with industrial partners and other academic collaborators, to constantly improve on the modeling and simulation system design, based on the evaluations of this phase of the project.
work and to start the process to layout a plan for the full development phase of the system design.

This project is a direct result of multiple-years of research experience on mixed signal systems and broadband (high-speed) communication systems. The preliminary implementation of these research experiences in several courses is our key objective in improving student learning.

3. Motivation

i) To introduce emerging technology into undergraduate teaching.

Some of the authors have taught communication systems lab and are very familiar with the mixed signal techniques lab. Both labs are very important labs within the electrical engineering curriculum. We have noticed that students are very seldom exposed to these emerging technologies in most of these labs in many Universities across the Nation. For example, both in the communication systems and in the mixed signal techniques labs, most of the emphasis in many Universities has been in the testing of various mixed signal and communication systems but not in the experimental modeling and simulation design of the systems. In this project, the experimental software system design of a low power, high-speed transceiver, chip-to-chip mixed signal communication system is used as a vehicle to introduce emerging technologies into undergraduate and graduate teaching.

ii) To bring experimental demonstrations into the classroom to assist student learning

Some of the authors have taught various undergraduate electrical engineering courses such as mixed signal techniques in design and testing, broadband (high-speed) communication systems, communication theory, signals and systems since 1984. One challenge we faced in teaching these courses was the lack of in-classroom experiments and demonstrations. It has been reported that a large percentage of engineering students are visual, sensing, and active learners according to Felder and Silverman [4] and it is necessary for them to see, touch and feel things before they can fully process engineering concepts according to Furman and Hayward [5]. Starting from 1999, one of the authors has been the founding Director of the mixed signal systems and high-speed (broadband) communication systems programs where he has developed fully functioning state-of-the-art labs that will be integrated to the demonstration and evaluation of this experimental modeling and simulation software design. Some of the authors have in all the classes they have taught since 1984 been given students class projects to link student intuition with theories which tends to significantly improve student learning. Due to the multi-functionality of this project, it has been used as a pilot program with the students in the Texas Instruments scholars program at Prairie View A&M University with successful results and can now be extended to other classroom courses.

iii) After a review of products from manufacturers of communication systems, very limited low power, high-speed transceiver, chip-to-chip mixed signal communication systems can be found. The use of transceivers in modern communication systems is an imperative and a burgeoning
area of focus for various military, consumer and industrial applications. The integration of mixed signal devices on a high-speed platform, which has the capability to reduce Inter Symbol Interference (ISI), signal distortion and maximize bits recovery rates, is the way forward to miniaturizing most communication applications while increasing their efficiency and reducing cost. These factors motivated the authors to work towards developing in the future a commercially available low power, high-speed transceiver, chip-to-chip mixed signal communication system.

4. Specification

The specification that can be deduced from the theoretical basis of this work that will assist student learning and undergraduate teaching includes:

i) Design of a high-speed serial transmission between ICs reduces both the number of IC pins and PCB tracks.

ii) For a given transfer rate, a multilevel signaling (8-PAM) scheme in system reduces the channel symbol rate to one third of that of a conventional 2-PAM transceiver.

iii) This symbol rate reduction lowers both the intersymbol interference (ISI) in the channel and the maximum required on-chip clock frequency.

iv) In the Data Transceiver System, the receiver oversamples with three fully differential 3-bit ADCs. The dataflow will transmit up to 1.3 Gb/s.

v) The transmission will be tested, measured and analyzed according to bit error rate of pattern bit sequence transmission, to evaluate the performance of the prototype

5. System Architecture

Figure 1 shows the block diagram of the transceiver operational chip-to-chip architecture system. In the low power, high-speed transceiver, chip-to-chip mixed signal communication system design, the transmitted data is digital, which is processed by means of DAC and ADC for transmission purposes, from which the received data are collected at the receiver end after error correction has taken place.

![Figure 1: Showing Basic Block Diagram of Transceiver Operational Subsystems](image-url)
Transmitter pre-emphasis is implemented without an increase in DAC resolution or digital computation. The receiver oversamples with three fully differential 3-bit ADCs. From the three samples, the one that is determined to be closest to the center of the data eye is selected as the recovered data. Baseline and gain compensation are performed in the receiver. The transceiver contains a 3-bit fixed pattern generator, a pseudorandom bit sequence (PRBS) generator, and a verifier for built-in self-test (BIST) according to Foley and Flynn [2].

The transceiver also incorporates a delay-locked loop (DLL)-based clock synthesizer that generates clock phases running at three times the reference frequency for the three receive ADCs. One of these clock phases also activates the transmitter. The DLL is self-correcting; it will not false lock to a multiple of clock periods. The circuit does not require the delay control voltage to be set on power-up. It can recover from missing reference clock pulses, and because the delay range is not restricted, it can accommodate a variable reference clock frequency. This allows the transceiver to be used for a wide range of data frequencies. The synthesizer has a measured rms jitter of 3 ps for a 500-MHz output frequency.

The transceiver can transmit up to 1.3 Gb/s and has a measured bit error rate (BER) of less than $10^{-13}$ for an 810-Mb/s PRBS transmission. The device, packaged in a 68-pin ceramic leadless chip carrier (CLCC), is implemented in 0.5µm digital CMOS, occupies 2 mm, and dissipates 400 mW from a 3.3-V supply. This circuit compares favorably in terms of reduced area to [6] (1 Gb/s, 0.5µm CMOS, 450 mW, 4 mm ) and [3] (8 Gb/s, 0.3- m CMOS, 1.1 W, 4 mm ) [2]. In our current work, we have focused on the modeling and simulation of the chip-to-chip transceiver system with the specified parameters discussed in this section. In Section 6, we will discuss the modeling and simulation work done.

6. Software Design Implementation

The software implementation of the architecture given in Figure 2 is done in this research project. Using MATLAB Simulink, we used a 3-bit Binary Weighted DAC and 3 flash ADCs using the complex process of data selection to process and correct received data. The modeling and simulation of the simplified 8-PAM Transmitter is shown in Figure 3. As shown in Figure 3, the input transmitted data are supplied by a random stepwise function generator and a word generator that are ‘muxed’, sampled and converted to their continuous form [7]. The data are then transmitted and received on the ADC side and the error samples generated and evaluated at the output signal (received data). The whole process is controlled by the DLL synchronized clocks. A built-in self-test platform is introduced to compare the data transmitted after the mux bus and the output obtained at the receiver end. Figure 4 shows the modeling and simulation of the simplified 8-PAM receiver system. Figure 5 shows the MATLAB-based simulated blocks implemented in this project.
Figure 2: Block Diagram Showing Software Implementation of the 8-PAM Transceiver.

Figure 3: 8-PAM Transmitter
Figure 4: 8-PAM Receiver

Figure 5: Simulation Block on MATLAB Simulink Showing Major Blocks
7. Hardware Design Implementation

On completion of the modeling and simulation design work, as part of our future work, the hardware system would then be implemented with the help of our industrial partners. As suggested in [8], the physical layout of the design is expected to consume 400 mW from a 3.3-V supply for a 1-Gb/s transmission over 15 cm of PCB track. The transceiver is intended to be fabricated on a generic 0.5µm triple-metal single-poly digital CMOS process and has an estimated die area of 2 mm [1, 2, 8].

8. Preliminary Results

Some preliminary work has been done on this project with good results. The simulated 8-PAM transceiver was able to achieve a maximum transmission speed of about 1 Gb/s. The transmitted data was nearly fully recovered, with ISI minimized and bit error rate reduced. With about 700-750 Mb/s, no error was detected. However, the simulation tends to be more accurate using a phase locked loop synchronized (PLL) source. 80% of the theoretical performance analysis was carried out, and the achievement level was nearly 90%. Jitter rate evaluation was not carried out. Figure 5 shows the simulation block on MATLAB Simulink showing the major blocks of the entire system. The simulation time was for about 10 seconds with speed of about 0.4 Gb/s and a BER that is less than 0.01. Figure 6 shows the 3-bit signal with noise (Transmission Data + Noise) while Figure 7 shows the PRBS verifier scope showing the receiver data bit error rate of 0.4 Gb/s. Figure 8 is the expected data acquisition results and Figure 9 is the Simulink output results.

Figure 6: Graph showing the 3-bit Input Signal with Noise (TxData + Noise)
9. Lessons Learned and the Integration with Teaching

Some of the issues encountered in the project are as follows:
- Some of the elements are not located in MATLAB (i.e. analog comparators, PRBS generator, resistors).
- We could not verify block models in Simulink.
The comparators in Simulink are code driven, not analog. Even with some of these issues, we were able to digitize a sine wave and compare it with an expected output shown in Figure (8 & 9). Table I shows the detailed information about integrating the low power, high-speed transceiver, chip-to-chip mixed signal communication system experimental modeling and simulation of the system design project with teaching in three diversified higher education institutions representing two-year, M.S.-granting, and Ph.D. granting university/college.

Table I: Integration of the Low Power, High-speed Transceiver, Chip-to-chip Mixed Signal Communication System Experimental Design Project with Teaching

<table>
<thead>
<tr>
<th>Institution</th>
<th>Type</th>
<th>Course Title/Instructor, Department</th>
<th>Level</th>
<th>Enr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prairie View A&amp;M University (PVAMU)</td>
<td>Ph.D. granting, Research University</td>
<td>ELEG 4273 Analog and Mixed Signal Techniques I (U); ELEG 4393 Analog and Mixed Signal Techniques II (U); ELEG 4313 Broadband Communication Systems I (U); ELEG 4323 Broadband Communication Systems II (U); ELEG 4473 Senior Design and Professionalism I (U); ELEG 4483 Senior Design and Professionalism II (U); ELEG 4291 Mixed Signal Testing Techniques Lab, ELEG 6243 Advanced Broadband Communication Systems (Gr.); ELEG 6553 Advanced Mixed Signal Systems (Gr.).</td>
<td>U/Grad.</td>
<td>200</td>
</tr>
<tr>
<td>Central Connecticut State University (CCSU)</td>
<td>M.S. granting, Majority</td>
<td>CET 402-Topics in Computer electronics Technology (U/Grad); CET-346 Signals and Systems (U); CET-443 Electronic Communications(U/Grad.).</td>
<td>U/Grad</td>
<td>125</td>
</tr>
<tr>
<td>Cy-Fair Community College (CCC)</td>
<td>Two-year</td>
<td>Summer Workshops for CCC students at PVAMU learning, doing research, designing in the areas of mixed signals and high-speed communication systems and participating in project.</td>
<td>U</td>
<td>10</td>
</tr>
</tbody>
</table>

Notes: U: Undergraduate, Grad.: Graduate, Enr.: Expected Enrollment,

Our industrial partner, Texas Instruments (an industrial leader in mixed signal systems, high-speed communication systems (broadband) and DSP solutions products) will evaluate this Low Power, High-speed Transceiver, Chip-to-chip Mixed Signal Communication System Experimental Design Project from technical and design perspectives and explore the possibilities for hardware implementation and commercialization. We have found out that the concepts developed here can be extended to both undergraduate and graduate courses as shown in Table I.
In the ELEG 4273, 4291, 4293 6553 mixed signal courses the students are taught the theories of ADCs and DACs and the necessary measurement techniques that can be implemented. In ELEG 4313, 4323 and 6243 Broadband communication systems, the students are taught all aspects of chip-to-chip high speed communication systems and theories. In ELEG 4473 and 4483, students implement what they have learned as a senior project course. In the courses taught at Central Connecticut University, they follow the same pattern in teaching their students. In the Community College, the intent is to bring selected students during the summer and train them using the research projects developed as a result of the work in the act of research and have them learn by implementing several aspects of the project.

10. Evaluation Plan and Lessons Learned

We intend to conduct surveys that can provide feedbacks regarding the effectiveness and to demonstrate the underlined concept of the design project. The survey results we intend to use to evaluate this project. Additionally, to review and compare our techniques, more surveys and interviews will be conducted throughout the project period as suggested in [9]. The objective of the questionnaire and the evaluations is to compare the ease-of-use and effectiveness of the system modeling and simulation results and then make decisions for hardware-based experiments at both universities. The metrics of evaluation will be ease of installation, ease of configuration changes, ease of adding new mechanisms, etc. We hope to identify their respective advantages and then use the results to map out a unified approach that might emerge. The following factors can be common to the studies across the universities:

- In addition to regular faculty evaluation, every class in which Mixed Signal Communication Systems related courses are taught, surveys can be administered at the beginning of the semester, and again at the end, in order to measure student progress.
- All instructors in these classes can use the Teacher Training materials, and all teaching assistants (TA) in these classes will use the TA Training materials.
- Instructors will use and comment on the lecture and lab materials prepared by the researchers. The material can be enhanced based on feedback obtained during the studies.
- Instructors will communicate with each other via the Co-Web website.
- Each university can record and analyze the following indicators to assess the effectiveness of the prepared materials:
  - Pre- and post- class survey results.
  - Collection and evaluation of student work using a locally designed rubric.
  - Follow-up observations of classroom implementation of curriculum materials.
  - Surveys of impact on student and teacher technical skills as a form of regular faculty evaluation.
  - Ongoing analysis by an evaluation team from institutions with common interest to refine program implementation.
  - Data collection on teacher training and TA training participation.
9. Conclusion, Recommendations and Future Work

Our preliminary results has shown that a high-speed 8-PAM modeling and simulation transceiver system can be implemented using the MATLAB Simulink software and the performance measures involving maximum speed, bits error rate and recovery speed can be verified in line with the theoretical limits obtained from a previous research. We have shown that this project as developed can be very instrumental in Electrical Engineering and Engineering Technology Departments in exposing our students to hands-on modeling and simulation training. In addition, the project as developed has the potential of given students the opportunity to design, develop, train and conduct tests in the broadband (high-speed) communication and mixed signal systems laboratories and the other various labs associated with the other disciplines and courses discussed in the paper. The lessons learned and recommendations are important to consider as discussed in this paper.

The next step for our future is the hardware implementation of this work and fabricates the low powered 8-PAM transceiver. The software allows the user to define dimensions; select from a broad range of device types and allows for simulated performance tests based on parameters already defined in the software implementation.

After the PC Lab design is completed and testing on this platform completed, the fabrication phase can then be done. It is recommended that most of the various disciplines in electrical engineering can work together to achieve the purpose desired in the future. Disciplines involved would include students from Mixed Signals, Communications, Microelectronics, IC Fabrication as well as Electronics and Materials Engineering. Thus, this is an all-encompassing project that would involve a broad range of disciplines as shown in Figure 10.
Experimental Design of a Low Power High-Speed Transceiver Chip-to-Chip Mixed Signal Communication System

Figure 10: Showing Possible Inter-Disciplinary Interaction in the Project Execution

References:

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