AC 2007-1208: TEACHING FIELD PROGRAMMABLE GATE ARRAY DESIGN (FPGA) TO FUTURE ELECTRICAL ENGINEERING TECHNOLOGISTS: COURSE DEVELOPMENT

Nasser Alaraje, Michigan Technological University

Joanne DeGroat, Ohio State University

Aurenice Lima, Michigan Technological University

Teaching Field Programmable Gate Array Design (FPGA) to Future Electrical Engineering Technologists: Course Development

Abstract

FPGA-based re-programmable logic design became more attractive during the last decade, and the use of FPGA in digital logic design is increasing rapidly. The need for highly qualified FPGA designers is increasing at a fast rate. To respond to the industry needs of FPGA designers, universities are updating their curriculum with courses in FPGA logic design. As a result, the School of Technology at Michigan Technological University is stepping up to this challenge by introducing the FPGA design course.

The new course will be the third in series of digital logic design, it introduces the students to techniques needed for the design of very-large scale digital systems, including computers basic building block. The paper discusses the goals of this course and relates the goals to industry needs of highly trained FPGA designers.

1 Introduction

The applications utilizing FPGA (Field Programmable Gate Array) as a design medium are predominant [1]. FPGAs have been used extensively not only in logic emulation but also in custom-computing machines. The re-programmability nature of SRAM-FPGA makes it the workhorse of many new reprogrammable applications. One such example is in multi-mode hardware applications [4] where an FPGA with a set of different configuration files stored in a ROM can be used to support different functionalities. Also, multiple-FPGA systems are used extensively in logic emulation.

SRAM-FPGA's are the most popular and becoming the workhorse of many re-programmable applications. SRAM - FPGAs' re-programmability feature makes it more attractive since it can be completely changed by the same electrical process. A microprocessor can be configured to run different applications, the configuration of SRAM-FPGA can be changed for bug fixes or even upgrades, this makes them an ideal prototyping medium. FPGAs have evolved from only a glue logic device to platform-based design medium. According to ITRS, we are approaching a four billion transistors chip by the end of this decade, this will allow building a very complex, high performance systems on FPGA.

As the technology scaling continues, more and more logic will be available on chip, this creates a great avenue for System-on-FPGA (SoFPGA) that provides the platform for (Intellectual Property) IP Cores re-use. IP Core can be either a hardcore or softcore. For example, Xilinx Virtex-II Pro is incorporated with IBM PowerPC hardcore RISC processors [9]. On the other hand, soft IP Core represents a more flexible synthesizable core that can be used on as needed basis.

Platform FPGAs will dominate the embedded system design in the near future [8], the capability to use a single programmable device that include a processor, interfaces, and programmable logic makes them the design of choice especially as price of FPGA comes down which will shorten the development cycle and reduce the time-to-market (TTM) pressure. As FPGAs become more widely used, the need for highly qualified FPGA designers is increasing at a fast rate. To respond to the industry needs of FPGA designers, universities are updating their curriculum with courses in FPGA logic design.

The paper first describes the motivation behind the development of this course in section 2 followed by the course objectives in section 3. In section 4, the course structure is presented. In section 5, the proposed course evaluation and instruments followed by paper conclusions in section 6.

2 Motivation

The main motivation for developing the new course was to respond to the market needs of skilled FPGA designers and as a result of consultation with the program industry advisory board, where one of the members of the industry advisory board is a representative of Lattice Semiconductor, the third market leader of programmable logic. As a result, the School of Technology at Michigan Technological University is stepping up to this challenge by introducing the FPGA course, the course major objectives are to give the students of Electrical Engineering Technology program the opportunity to learn and experience logic design using FPGA. This will create a pool of informed electrical engineering technologists from which industry can draw their potential staff. This common pool of students will be given the opportunity to conduct research in FPGA Design.

The FPGA design course will be the third in digital logic design series courses. In developing the new FPGA design course, one of the key factors was to have a course that would match the industry expectation of qualified FPGA designers with extensive hands-on experience with industry widely used design tools. The EET program offers hands-on laboratory experiences which contribute significantly to students' success.

3 Course Objectives

Due to increase demand of FPGA designers, the intention of this course is to give students a real-world experience on FPGA logic design and give them the necessary training with industry widely used design tools, XILINX ISE webPACK, ModelSim simulation tool, and FPGA design implementation on XILINX SPARTAN FPGA evaluation board. The long term objectives of this course is to provide a learning opportunity at the School of Technology which will result in a research activities focused on FPGA design, this research would provide more in-depth training for senior students and engage undergraduate students in applied research opportunity at SoT.

The academic objectives of FPGA logic design course are to provide students with skills and experience that will help them to be attractive in job market. The students will learn the design of major components of digital systems, such as arithmetic logic units (ALUs), floating points, memory, and controller using hardware description language (HDL), the students will learn FPGA design flow starting from HDL design entry, circuit simulation to verify the correctness of the intended design, followed by FPGA Synthesis, Place and Route and timing analysis. To accomplish this in one semester course, the intent of lectures and labs is to have the students:

1. Learn the design of major components of computer architecture.
2. Learn fundamental concepts of hardware description language.
3. Learn how to use HDL for modeling basic building blocks of digital system.
4. Students will learn FPGA technology and impact of using FPGA in logic design.
5. Learn FPGA design flow using XILINX ISE webPACK and modelSim simulation tools. Students will gain FPGA design experience to synthesize, map, and place and route a given design on XLINX SPARTAN FPGA evaluation board.
6. The students will work in groups of two to three and thereby learn how to cooperate in teams and also document their results.

The designs are carried out using modern computer-aided design (CAD) tools. The final systems will be implemented with state of the art devices such as Xilinx FPGA device family and micro-controllers. XILINX SPARTAN3 evaluation boards will be used as the target platforms, these boards were donated by XILINX as well as the XILINX ISE webPACK development tools.

4 Course Structure

The course "Topics in Programmable Logic" developed at the School of Technology at Michigan Technological University is three credit hours with two hours per week of recitation and a three hour lab part. The course will be open for senior students and the pre-requisite is EET2142 "Digital Design and Modeling using VHDL"[1], this course will be the third in digital logic design series. The course will integrate XILINX ISE webPACK and ModelSim from Mentor Graphics. The lab will be using Xilinx Spartan family evaluation boards, the FPGA boards will be used as target platforms for lab experiments. Student will learn how to implement a complete system on the FPGA evaluation boards.

Each FPGA vendors provides software development tool that has its own features, the most widely used is Xilinx ISE webPACK [2] since Xilinx represents the market leader and gains the largest market share compared to Altera, the second leader in programmable logic design. Each design tool is device dependent and Xinlinx ISE webPACK only target Xilinx device family. Learning ISE webPACK will give the student the opportunity to learn FPGA design flow using the most widely used tools for FPGA design, at the same time, these skills are transferable to other design tools.

5 Course Evaluation & Assessment Instruments

The course evaluation is based on two one-hour midterms that represents 40% of total grade, the two midterms will be the assessment instruments for course objectives (1), (2), (3), (4), and (5). On the other hand, the lab assignments represent 30% of the total grade and will be used as the assessment instrument for course objectives (1), (2), (3), (4), (5) and (6) . Final Exam will be given at the end of the semester and represents 20% of the total grade, the exam will be used as the assessment tool for course objective where the students will be expected to demonstrate their mastery of knowledge. The final exam will be used as the assessment instruments for course objectives (1), (2), (3), (4), and (5).

The lab assignments will be the important components of the course and measure the hands-on design experience. On the other hand, the lecture will cover:

- Concepts of hardware description language modeling of common components of digital system.
- Tutorial on the design development tools, the XILINX ISE webPACK and ModelSim.
- FPGA Architecture which covers topics in Configurable logic blocks (CLB), on chip wiring, memory hierarchy such as Lookup Table (LUT), Block RAM, and IO Blocks.
- FPGA Design Flow which covers the design entry followed by technology Synthesis and Place and Route.
- Xilinx EDK both structure and programming which covers a VHDL soft processor, Busses, GPIO, UART, Software debugging, building a system in the SPARTAN device.

The course will enable students to gain real-world experience and contribute to FPGA based research project.

6 Conclusion

With the demand of skilled FPGA designers on the rise, the objectives of this paper was to present "Topics in Programmable Logic" course, which will be a new addition to the electrical engineering technology program at School of Technology. The course offers students a real-world experience in FPGA based logic design. This will create a pool of informed electrical engineering technologists from which industry can draw their potential staff. This common pool of students will be given the opportunity to conduct research in Field Programmable Gate Array (FPGA) Design.

The first offering of the course will be in spring 2007. The goals of this course is to give students a real-world experience on FPGA logic design and give them the necessary training with industry widely used design tools, XILINX ISE webPACK, Xilinx Spartan Family Evaluation board and ModelSim simulation tool. On the other hand, the long term goals of this course is to provide a learning opportunity at the School of Technology which will result in a research activities focused on FPGA and hardware design modeling. This research would provide more in-depth training for senior students.

References:

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