

Testing the Susceptibility of a High-Speed Integrated Circuit

Ludovic V. Grivault, Matthew J. Gualdoni, Daryl G. Beetner

Electromagnetic Compatibility Laboratory, Missouri University of Science & Technology

Abstract

High-speed integrated circuits (ICs) can be very sensitive to electromagnetic interference. If the response of the circuit to electromagnetic interference can be quantified and understood, the circuit – or the system it goes in to – can be made more robust and reliable. The following paper outlines the development of hardware to allow testing of an SRAM module against electromagnetic noise. The ultimate goal of the work is to develop models which predict the susceptibility of digital ICs.

Motivation

Models of the electromagnetic immunity of digital ICs could help the IC designer build better ICs and help the board designer build better systems that use these ICs, but unfortunately such models are not widely available. A test IC containing components common to all digital ICs was built to help develop immunity modeling strategies (Figure 1). One component in test IC is an SRAM circuit, which requires many digital signals to properly read and write values from memory. A method was needed for generating and reading the digital signals to and from the FPGA at high speeds. Digital signals were generated with a Cyclone III FPGA development board with an external clock speed of 50 MHz. The switching frequency of the signals had to be around 400 MHz, which is faster than the internal clock.

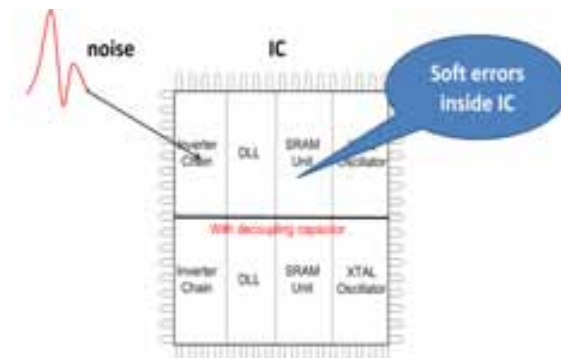


Figure 1. Overall architecture of the test IC.

Initial Solution

The first attempt to get very fast signal speeds was to use the logic gates delays to build signals faster than the clock – essentially creating signals using glitches in the logical circuit (Figure 2). While this method works, it is inflexible and challenging to implement, since any changes to the signal requires the creation of a new custom circuit.

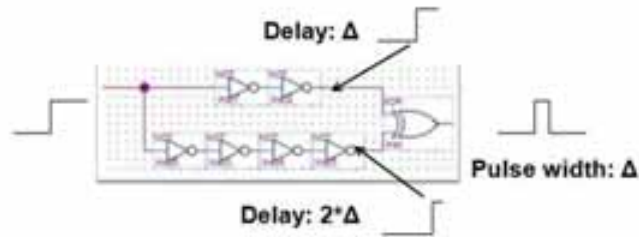


Figure 2. Faster-than-the-clock signals can be built using glitching.

Final Solution

The Altera Cyclone III FPGA¹ on the development board includes special-purpose LVDS transceivers. These transceivers are capable of generating signals of very high speeds – even faster than the clock. Special-purpose Megafunctions² are used to communicate with the transceiver. These Megafunctions allow the design and control of signals generated by the LVDS transceivers, enabling the FPGA to transmit the required signals. Since the IC on the test board can only receive single-ended signals, the LVDS transmitters were connected to a differential to single-ended converter to convert the differential LVDS signals to a single-ended, 0-5 V, format.

The six signals needed by the SRAM module were coded in VHDL. Simulations showed the output signals could be generated much faster than the 400 MHz requirement. A test board is currently being built that will allow hardware testing of the design.

The Team

The investigating team was comprised of a diverse group of students, which included undergraduates from Missouri University of Science and Technology and visiting undergraduates from ESIGELEC in Rouen, France. These students worked together with S&T graduate students to generate a working solution. This created a diverse work environment, and gave students experience collaborating as a member of a very heterogeneous group. The diversity at times created some communication issues, but overall the team greatly benefited from the different perspectives provided by the different educational backgrounds of the team members.

Accomplishments and Lessons Learned

The comparisons between the signal generation techniques using glitching and using the transceivers illustrates that we must take in consideration the reusability and the flexibility of the design. The result must be easy to maintain and modify. Later design of hardware transforming the LVDS signal to a single-ended TTL signal also emphasized the need to consider the limitations of all components in a design. Finding a comparator that could generate a TTL output as fast as the LVDS signal from the FPGA was challenging.

References

1. Altera corporation, “Cyclone III device handbook”, August 2012, available at http://www.altera.com/literature/hb/cyc3/cyclone3_handbook.pdf.
2. Altera corporation, “Introduction to Megafunctions, user guide”, November 2011, available at http://www.altera.com/literature/ug/ug_intro_to_megafunctions.pdf.

Testing the Susceptibility of a High-Speed Integrated Circuit

Ludovic V. Grivault, Matthew J. Gualdoni, Daryl G. Beetner
Missouri S&T EMC Laboratory

Introduction

High-speed integrated circuits can be very sensitive to electromagnetic interference. If the response of the circuit to electromagnetic interference can be quantified and understood, the circuit – or the system it goes in to – can be made more robust.

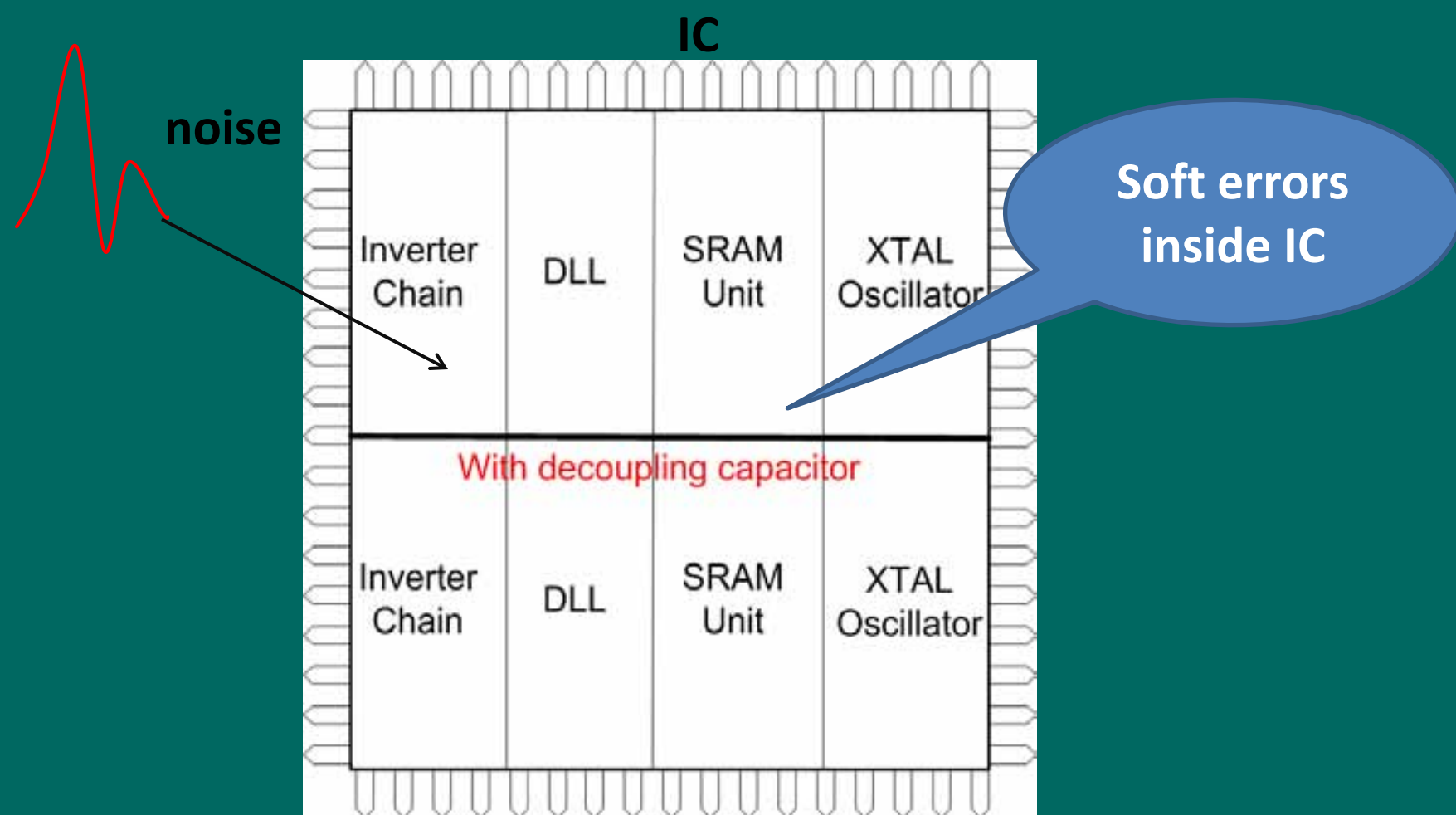


Fig. 1. Overall architecture of the IC.

A test chip was built to help develop models of IC immunity. Our team worked on the SRAM part of the IC.

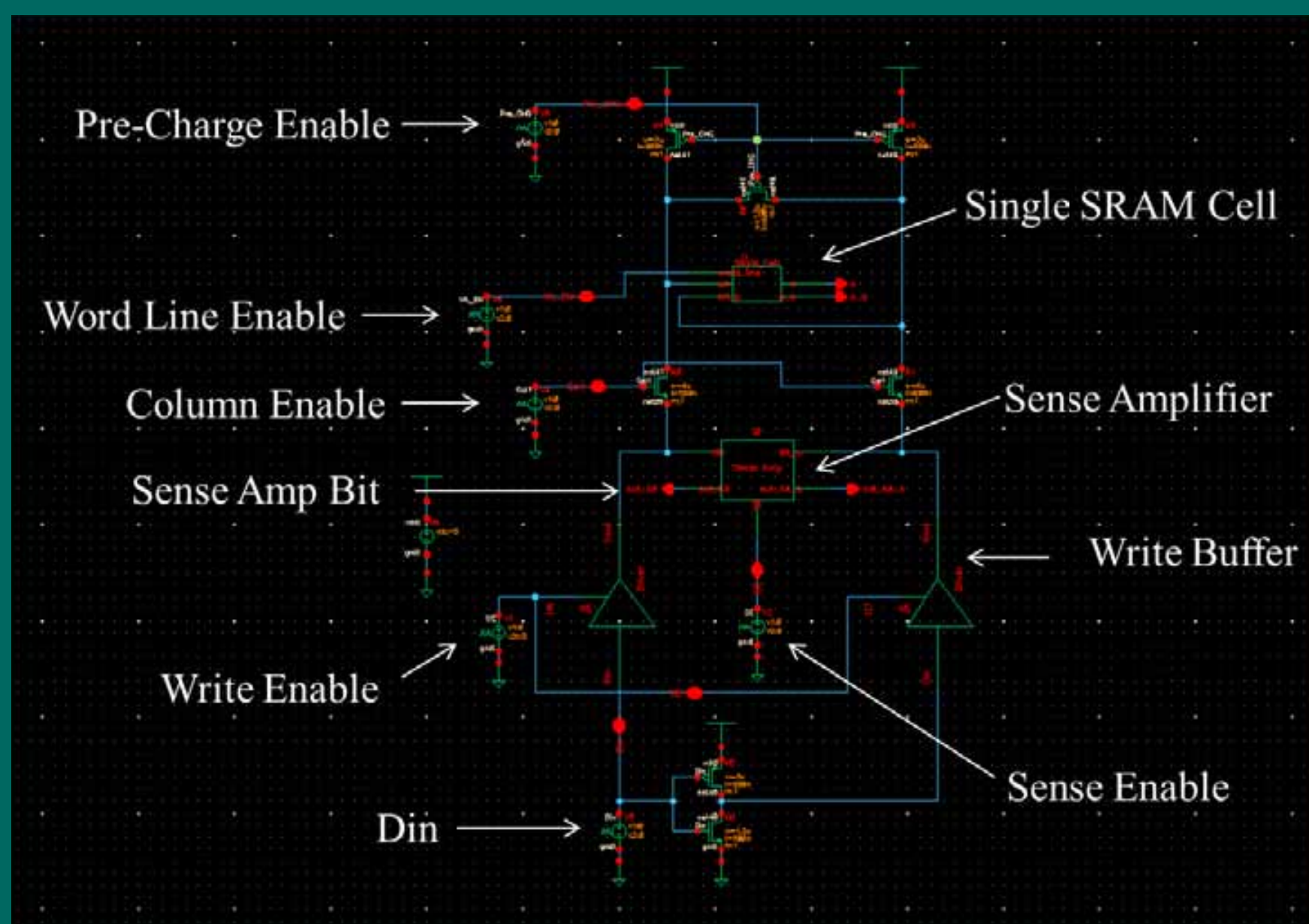


Fig. 2. SRAM module

A test board was developed to quantify the impact of electromagnetic noise on the test IC. The board had to be capable of transmitting high-speed digital signals. Digital signals were generated with a Cyclone III FPGA development board with an external clock speed of 50 MHz. The switching frequency of the test signals had to be at least 400 MHz. Specialized PLL functions provided by the FPGA were used to reach this frequency. These functions required the use of an LVDS transceiver, so a differential to single-ended converter also had to be used on the PCB.

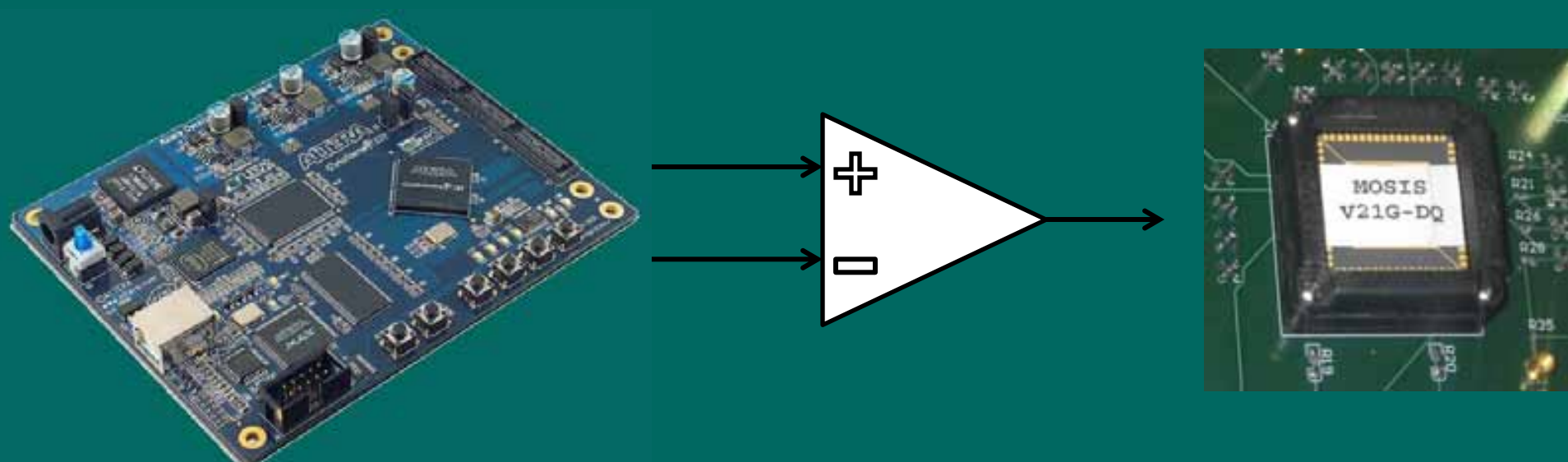


Fig. 3. Signal generation

First Attempt

The first attempt to get very fast signal speeds was to use the logic gates delays to build signals faster than the clock – essentially creating signals using glitching. While this method works, it is inflexible, since each signal requires a custom circuit.

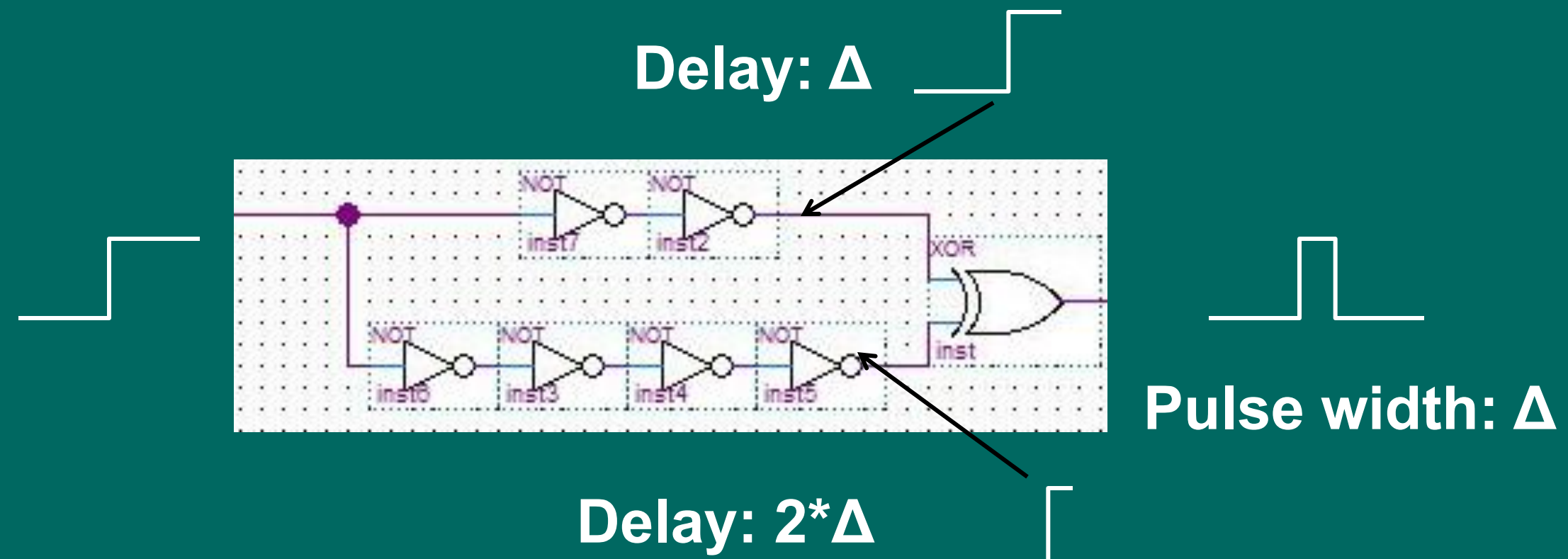


Fig. 4. Signals built using glitching

Final Solution

The Altera FPGA includes special purpose I/O transceivers that may operate faster than the clock. These transceiver megafunctions were used to generate the test signals.

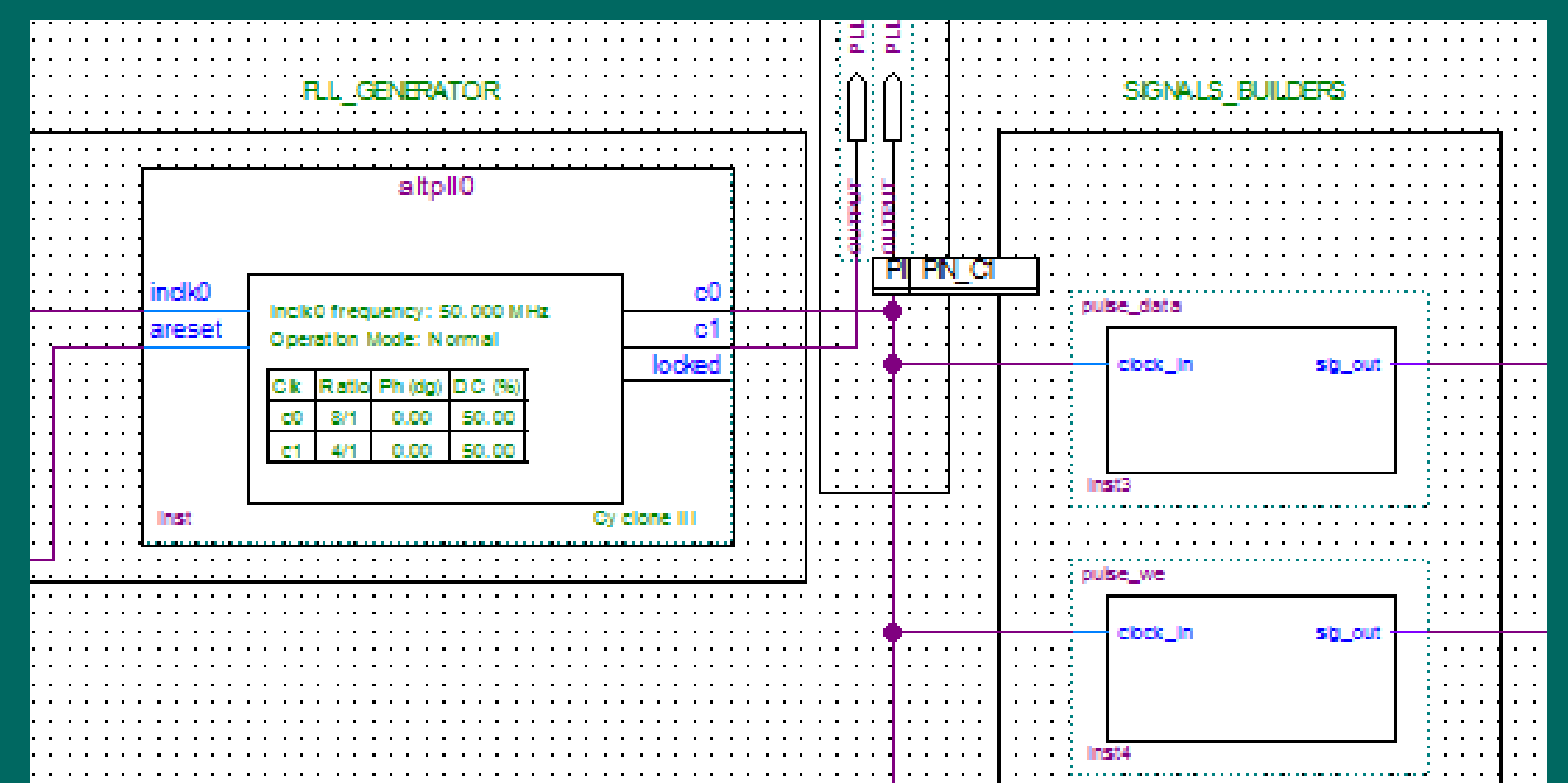


Fig. 5. VHDL implementation using Megafunctions

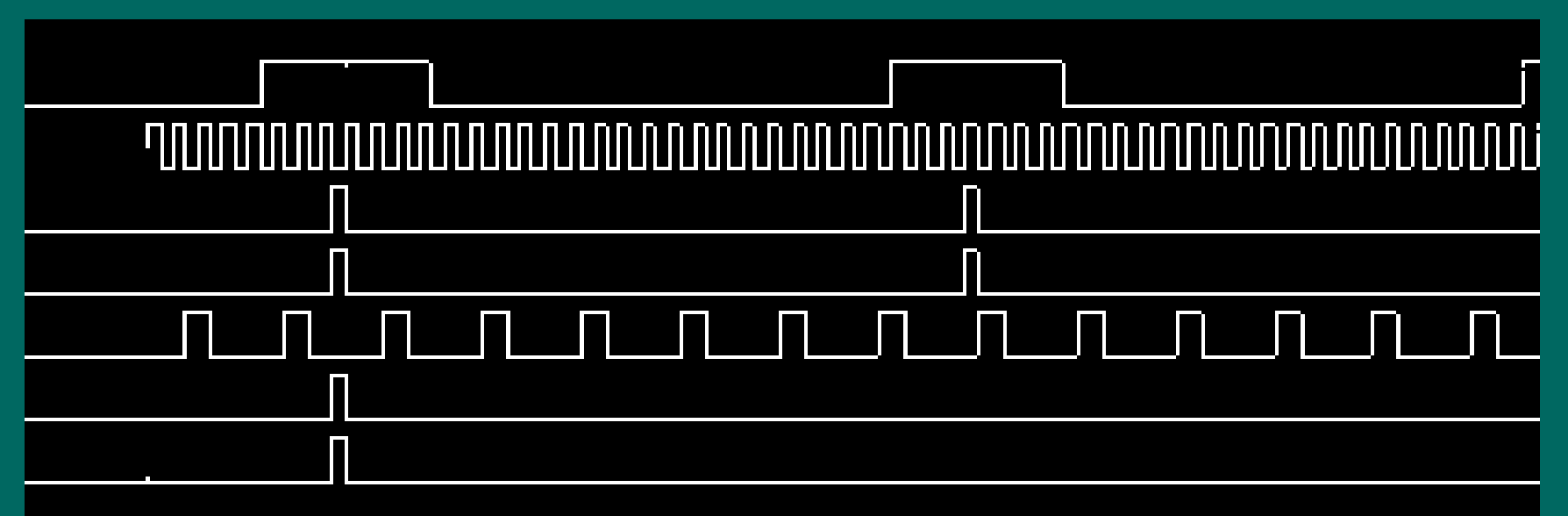


Fig. 6. Simulated output signals

The Team

The investigating team was comprised of a diverse group of students, which included undergraduates from Missouri University of Science and Technology and from ESIGELEC in Rouen, France. These students worked together with S&T graduate students to generate a working solution. This created a diverse work environment, and gave students experience collaborating as a member of a very heterogeneous group.

Conclusions

A circuit was built to provide faster-than-the clock signals for immunity testing of an SRAM module. The interaction between undergraduate and graduate students, French and English speakers provided an interesting twist to the educational experience.