The Motorola DSP56002 EVM, A Powerful Tool for Teaching Real-Time DSP

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Abstract
A senior undergraduate/first year graduate course in real-time digital signal processing(dsp) is described. The purpose of the course is to facilitate the learning of important dsp concepts and to equip students with the hardware/software tools and knowledge for designing real-time digital signal processing systems. Fixed and adaptive FIR digital filters are discussed and implemented. Spectral analyzing systems and a variety of student independent projects are undertaken. The course has proven to be a good preparation for the increasing industrial demand for entry level engineers with hands-on dsp know-how.

Introduction
The California State University, Chico(CSUC) offers Electronics Circuits for Digital Dignal processing, an undegraduate/first year graduate course, with two hours of lectures and three hours of laboratory per week. The course has as its objective, to facilitate student understanding of DSP concepts by implementing real-time applications, and develop appreciation for comparative VLSI DSP architectures by working with the Motorola DSP56002. The course, which has been taught about five times using the DSP56001 with good student response, is now being modified to use the higher speed(but architecturally equivalent) DSP56002. The textbook for the course is Mohammed El-Sharkawy's "Real-Time Digital Signal processing Applications with Motrola DSP56000 Family, Prentice-Hall, 1990. This text is supplemented by other readings from the literature.[1,2]

A digital signal processor(dsp) is a special purpose microprocessor whose internal computing circuits are tailored primarily to the predominant arithmetic process required in most digital signal processing applications. Dsp's have been the key components in today's commercial multimedia systems, such as speech, digital audio, and image processing. Key signal processing applications, such as digital filtering and the Fast Fourier Transform(FFT), entail the repeated multiplication of two entities, namely, a filter coefficient and an input signal sample. Powerful processors, such as the Motorola DSP56002, accomplish a multiply-accumulate('MAC') in one parallel step. Equations (1) and (2) below represent the Finite Impulse Response Filter(FIR) and the Discrete Fourier Transform(DFT) showing the 'MAC' nature of the operations.

The relationship between a FIR filter's digital input sequence x(n) and digital output sequence y(n) can be written as:

$$y(n) = \sum_{i=0}^{N-1} b(i)x(n-i) \qquad (1)$$

where b(i) are filter coefficients and N is the number of those coefficients.

The discrete Fourier transform, on its part, can be defined as:

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \qquad (2)$$

For a real or complex discrete-time sequence x(n) of length N, the summation in (2) above gives a complex frequency X(k) of length N. W_N^{nk} is known as the "twiddle" factor or the weighting factor.

Course Lecture Topics

The list of lecture topics treated in the course provided below:

1. Overview of real-time DSP laboratory facilities.
2. DSP56002 architecture and addressing modes.
3. DSP56002 instruction set and software design.
4. FIR filters and the DSP56002.
5. Fast Fourier transform and the DSP56002.
6. Adaptive filters, theory, applications and implementations.
7. Other applications of real-time DSP, multimedia, active noise cancelers.

Course Laboratory Exercises and projects.

During the first half of the semester, experiments are designed and run for real-time implementations of FIR and adaptive FIR filters, as well as FFT for implementing a spectrum analyzer. During the second half of the semester, students undertake short independent projects, some of which are subsequently expanded to become Senior projects or Masters Thesis. Representative projects have included a data scrambler/descrambler, sinewave generation, spectral analysis and adaptive filtering.

The FIR filter experiment involves two steps. First, using Motorola's published data on instruction execution timing for relevant dsp instructions and addressing modes of the DSP56002, detailed calculations are made to determine the number of clock cycles required to execute all the instructions for an FIR filter. The calculations are done for an FIR filter for a varying number of taps. Increasing the number of taps, or filter weights, improves the sharpness of filter cut-off characteristics. Filters with taps values ranging from 10 to 1000 and above are investigated.

The second step has to do with actual real-time implementations of the FIR filters with the varying number of taps as discussed above. The extraction of the filter performance characteristics is done by obtaining the real-time spectral response of the filter using a Fourier analyzer. A brief description of the experimental set-up is provided below.

Real-time filter implementations involve the following steps:

a) A commercial filter design package, the Momentum Data Systems' "QEDesign' package running on an IBM PC, is used to generate the filter coefficients.

b)An assembly language filter program is designed to perform filtering using the coefficients and the samples of an actual incoming signal.

c) The spectral characteristics of the output signal is compared to the spectral characteristics of the incoming signal in order to determine filter response characteristics.

The real-time filter implementations are performed on the 80 MHz Motorola DSP56002 24-bit fixed point dsp. The processor is the heart of the DSP56002 evaluation boards donated by Motorola Inc. Each evaluation board has a 16-bit high performance multimedia stereo audio

programmable codec. The codec is a Crystal Semiconductor Corporation's model CS4215 . The software development environment for the evaluation board is a powerful emulator incorporating a Microsoft Windows-based simulator. It also has a C, assembly, and mixed mode debugger with a graphical user interface providing up to 20 windows operating concurrently. Because of that, observation of multiple variables and detailed analysis of the instruction execution process can be made. A total of six evaluation boards and associated measurement equipment and software are set up to yield six laboratory stations. Therefore, with three students per laboratory group, a maximum of eighteen students are accommodated in a laboratory session.

Input signals to the filter are provided by an HP 3311A function generator or a Tektronix 2642A Fourier analyzer with capability for extracting transfer functions of systems. An HP 54600A two-channel oscilloscope is used to monitor input and output signals. The QEDesign filter design package by Momentum Data Systems Company is used for rapid filter design and analysis.

Variations on the FIR filter implementations include the design and implementation of a multi-band filter and its use to perform a graphic equalizer in the audio band.

The spectrum analyzer project entails the implementation of a 1024-point FFT with the DSP56002. The real-time results are displayed on an oscilloscope to show the discrete frequency components extracted from the input signal. Single tones, mixed tones and band-limited white noise are used as imputs to the system.

Conclusion

Our DSP students feel that the hands-on component makes a major positive impact on their understanding of basic DSP concepts. They have been very highly motivated by the laboratory component, and no longer view DSP as abstract and esoteric.

References

1. Kevin L. Kloker, "The Motorola DSP56000 Digital Signal processor", IEEE MICRO, Dec. 1986, P. 29-50.
2. Special Session on Signal processing Education, In proceedings, 1993 International Conference On Acoustics, Speech and Signal processing(ICASSP), Vol I p. I.4-I-36.

Biography

ALBERT O. RICHARDSON is Professor of electrical and computer engineering at the Californis State University, Chico, where he has been since 1989. He holds a B.S. from Yale University and a Ph.D from the Pennsylvania State University. His expertise is in digital systems and digital signal processing.