The Pressure Sensing Project

Nghia T. Le, Terry O'Connor
Purdue University
School of Technology
Electrical Engineering Technology

A. Introduction

The paper discusses the use of a multi-faceted electronic project as a capstone experience for an associate degree program in Electrical and Computer Engineering Technology (ECET) at Purdue University's School of Technology New Albany location. This project incorporates several different technologies from both the analog and digital realms of electronics. The project is designed by the course instructor of ECET 297 – Electronic System Design and Fabrication. ECET 297 is in the fourth semester of the A.S. program. The students are given the design of the circuit in block diagram and schematic form. Each subpart of the circuit is intended to provide review to the student as each technology has been covered in previous courses. The students are then required to fabricate the circuit one portion at a time until the project is completed. Fabrication of the project is done on prototyping (UBS-100) boards. Each section must be functioning correctly before the next section is to be fabricated and thus the project provides an excellent troubleshooting experience. Careful and neat layout of the circuit is mandated by the course instructor and the course grade is partially dependent on that. A project such as this one has been used each of the past six years in ECET 297 in New Albany. Each year's project is unique as the course instructor designs a new one for each successive class. The faculty in ECET at New Albany considers the projects used over the past six years in the course to have been effective capstone experiences for the students. Student feedback on this course has been excellent and individual students have reported that they have had such pride in their completed project that they have kept it fully assembled on its protoboard years after graduating.

The remainder of the paper discusses the design of the project. This project is a Pressure Sensing circuit that utilizes a variable capacitor as a pressure switch. The variable capacitor is constructed by using two conducting plates with a foam layer in between as in Figure 1 on the next page.

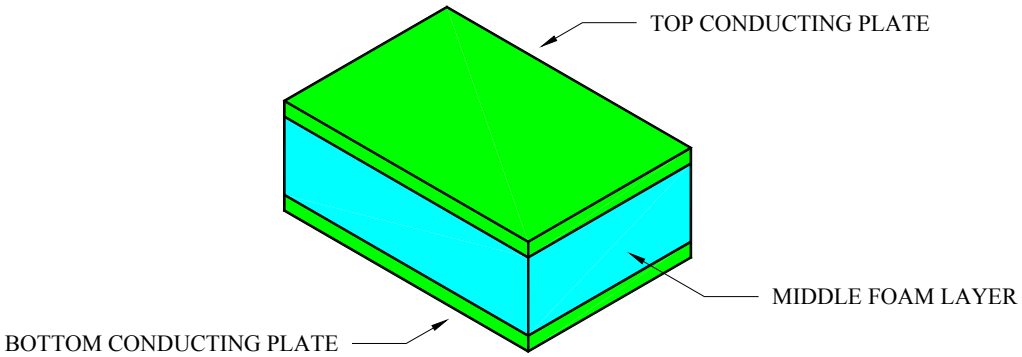

Figure 1 – The Variable Capacitor

When pressure is applied to the top plate, the foam layer collapses resulting in an increase in the capacitance. The project utilizes this behavior to sense the pressure presence. The design covers basic analog/digital circuits that the students learn during the first two years in the Electrical Engineering Technology Program at Purdue University. Figures 2 and 3 show the block diagrams of the project.

When the top plate is pressed down to 1/3 of the gap, the 3-digit display shows the time in seconds that the pressure is present. At the same time, the first LED is lit to show that the distance between the two plates has decreased 30%. If the pressure keeps increasing, the time continues to count and the second and third LED's show 60% or 90% when the gap reaches these points. When the pressure is released, the time freezes to show the total time the pressure has been presented. When the top plate is pressed down the second time at 30%, the time resets itself and starts counting again.

The project consists of different stages that are manageable as weekly classroom activities. It helps the students to utilize their knowledge to design and build a working circuit.

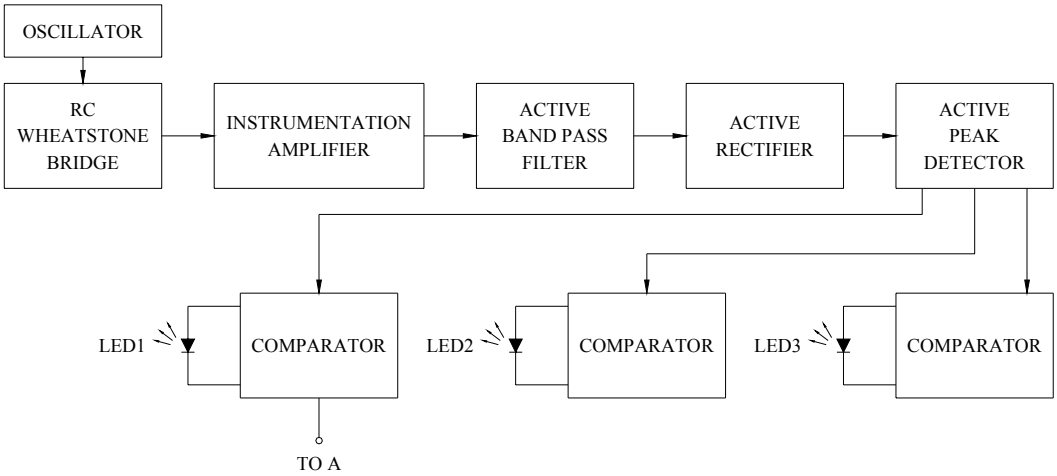

Figure 2 – The Analog Section of the Project

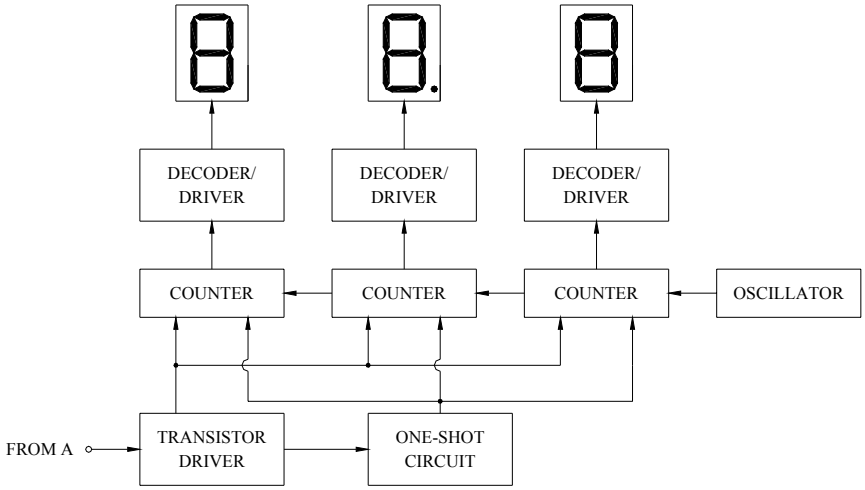

Figure 3 – The Digital Section of the Project

B. The Analog Section of the Project

1. The Wien-Bridge Oscillator

The schematic diagram of the Wien-Bridge oscillator is in Figure 4 below.

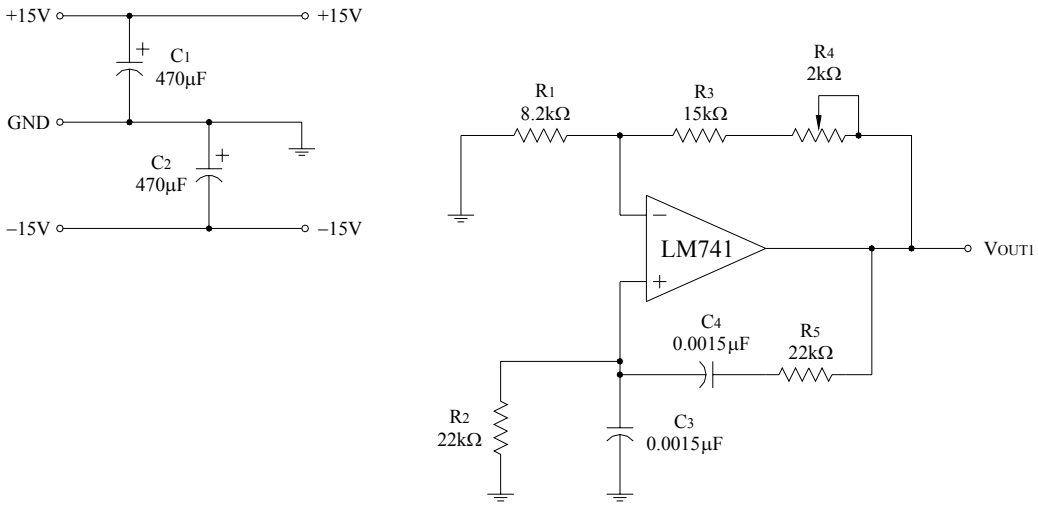

Figure 4 – The Wien-Bridge Oscillator

The ±15VDC power supply has two 470µF filtering capacitors as in the top left corner in Figure 4.

In the oscillator, if we let $R_2 = R_5 = R$ and $C_3 = C_4 = C$, the oscillating frequency is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi(22k\Omega)(0.0015\mu F)} = 4.82kHz$$

Let K be the closed-loop gain of the Non-Inverting amplifier section. In order for oscillation to occur, we need:

$$K = 1 + \frac{R_5}{R_2} + \frac{C_3}{C_4} = 1 + \frac{22k\Omega}{22k\Omega} + \frac{0.0015\mu F}{0.0015\mu F} = 3$$

Therefore,

$$K = 3 = 1 + \frac{R_3 + R_4}{R_1} \Rightarrow (R_3 + R_4) = 2R_1 = 2(8.2k\Omega) = 16.4k\Omega$$

In the design, a 2kΩ–22 turn rheostat is used for R_4 to fine-tune the circuit for oscillation.

The waveform of the output of the oscillator is in Figure 5 below.

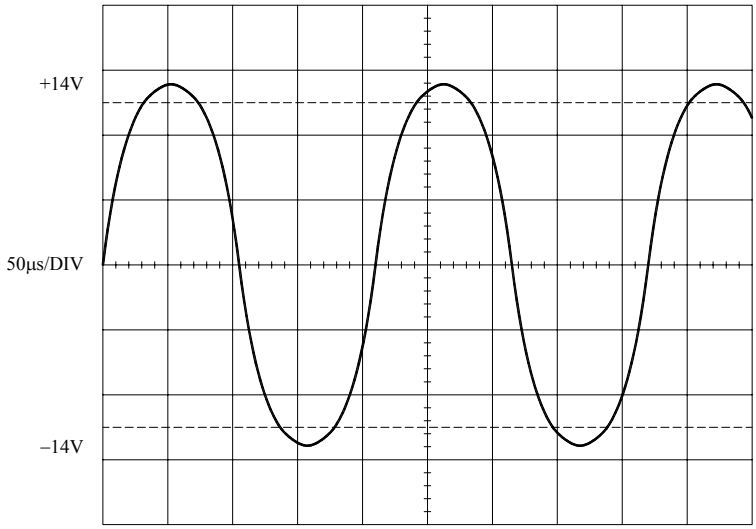

Figure 5 – The Oscillator Output

The output of the oscillator is the reference voltage for the following RC Wheatstone bridge circuit.

2. The RC Wheatstone Bridge

The schematic diagram of the RC Wheatstone bridge is in Figure 6 below.

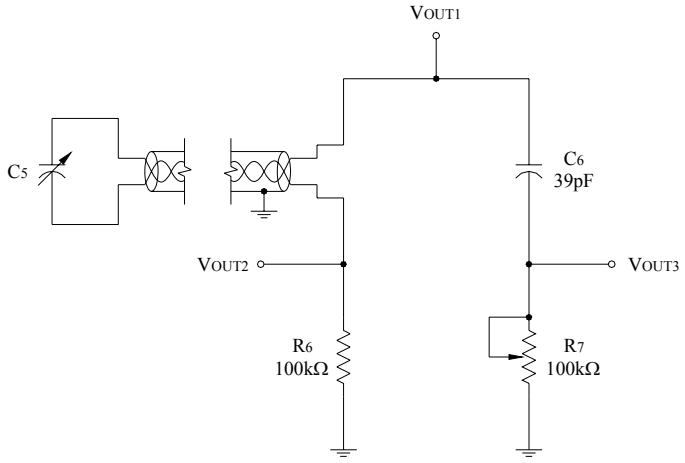

Figure 6 – The RC Wheatstone Bridge

The reference voltage of the bridge V_{OUT1} comes from the output of the Wien-Bridge oscillator. The variable capacitor C_5 is the pressure switch that is mentioned at the beginning of this paper. The 100kΩ–22turn rheostat R_7 is used to balance the bridge.

The outputs of the bridge V_{OUT2} and V_{OUT3} are the inputs of the following Instrumentation amplifier.

3. The Instrumentation Amplifier

The schematic diagram of the Instrumentation amplifier is in Figure 7 below.

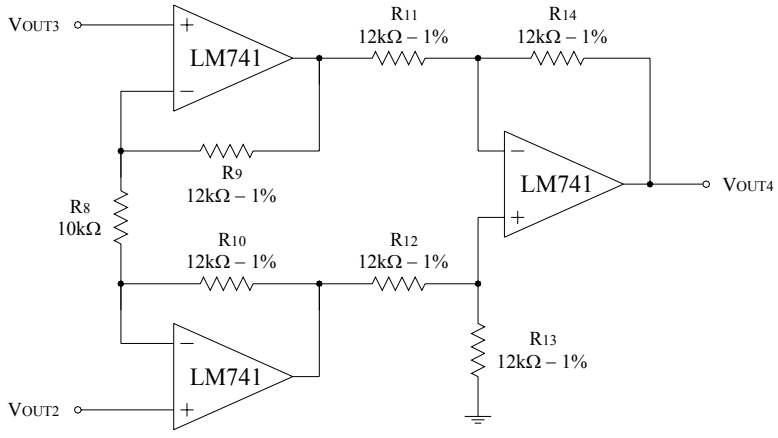

Figure 7 – The Instrumentation Amplifier

In the amplifier, if we let $R_9 = R_{10} = \ldots = R_{14} = R$, the output of the amplifier is:

$$V_{OUT4} = (V_{OUT2} - V_{OUT3})\left(1 + \frac{2R}{R_8}\right) = (V_{OUT2} - V_{OUT3})\left(1 + \frac{2(12k\Omega)}{10k\Omega}\right) = 3.4(V_{OUT2} - V_{OUT3})$$

Because of the phase shift between V_{OUT2} and V_{OUT3}, it is impossible to obtain a 0V output level for V_{OUT4}.

Table 1 below shows the peak values of V_{OUT4} at different pressure levels.

	Normal	First Level	Second Level	Third Level
$V_{OUT4\ PEAK}$	300mV	400mV	480mV	600mV

Table 1 – The Output Peak Values of the Instrumentation Amplifier

The waveform of V_{OUT4} under normal condition is in Figure 8 below.

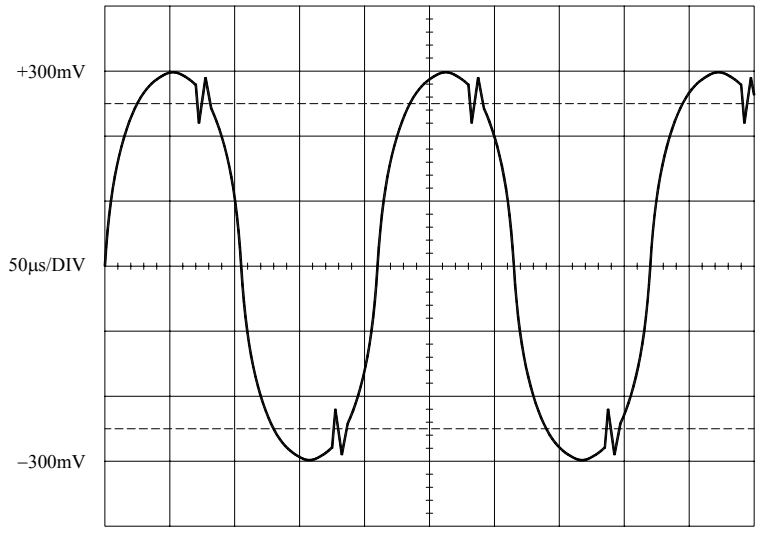

Figure 8 – V_{OUT4} Under Normal Condition

Since the above output is not a perfect sinusoidal wave, we need to condition the waveform and to amplify the signal by using a Second Order Active Band Pass filter.

4. The Second Order Active Band Pass Filter

The schematic diagram of the filter is in Figure 9 below.

In the circuit, a Buffer is used to isolate the output impedance of the Instrumentation amplifier from the input impedance of the filter.

If we let $R_{15} = R_{17} = R_{18} = R$, and $C_7 = C_8 = C$, the center frequency of the filter is:

$$f_0 = \frac{\sqrt{2}}{2\pi RC} = \frac{\sqrt{2}}{2\pi(12k\Omega)(0.0039\mu F)} = 4.81kHz$$

The above center frequency matches with the oscillating frequency of the Wien-Bridge oscillator.

Let K be the closed-loop gain of the Non-Inverting amplifier section, we have:

$$K = 1 + \frac{R_{19}}{R_{16}} = 1 + \frac{33k\Omega}{12k\Omega} = 3.75$$

The sensitivity value of the circuit is:

$$Q = \frac{\sqrt{2}}{4 - K} = \frac{\sqrt{2}}{4 - 3.75} = 5.7$$

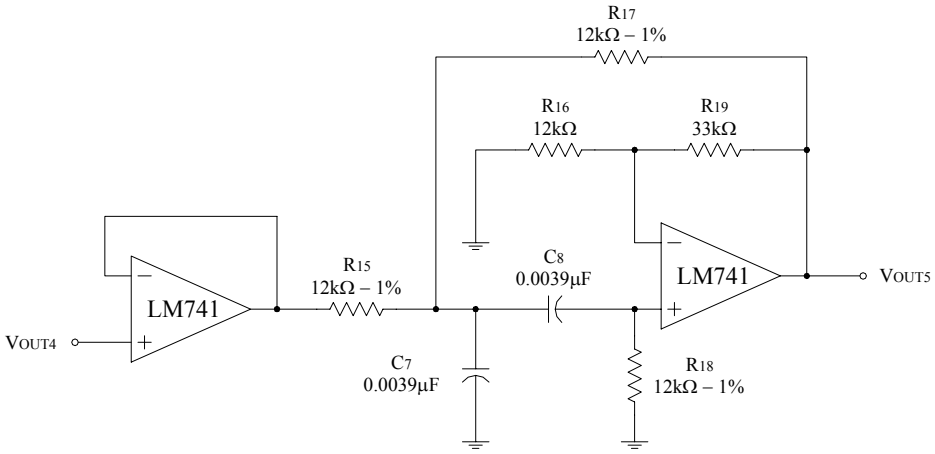

Figure 9 – The Second Order Active Band Pass Filter

Proceedings of the 2004 American Society for Engineering Education Annual Conference & Exposition

Figure 10 below shows the output waveform of the filter under normal condition.

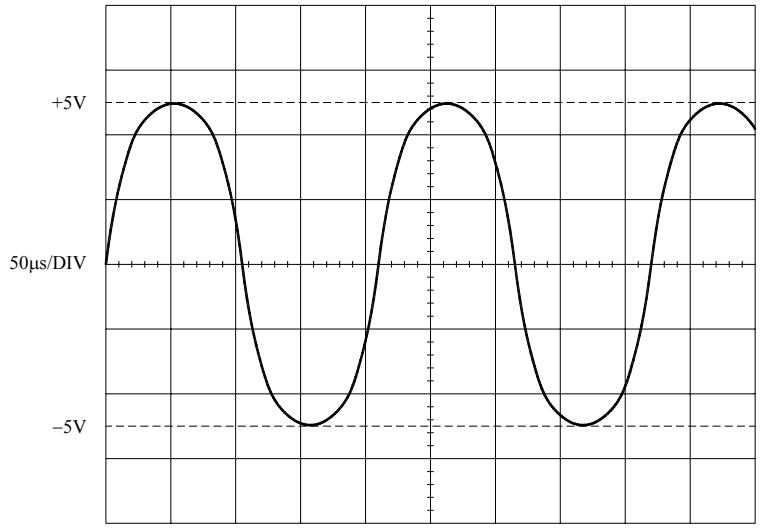

Figure 10 – The Output Voltage of the Band Pass Filter

Figure 11 below shows the frequency response of the filter with a 600mV-peak input signal.

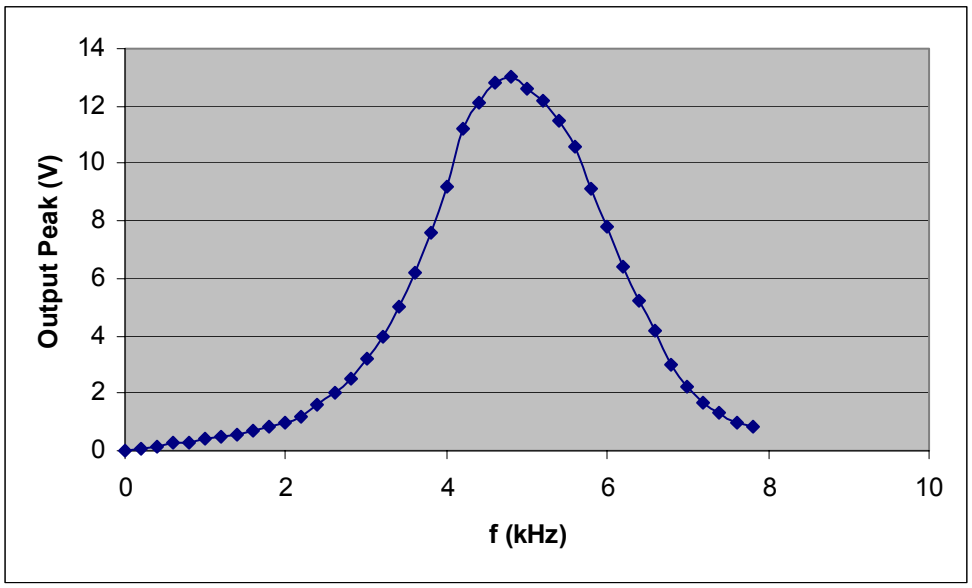

Figure 11 – The Band Pass Filter Response

Table 2 below shows the peak values of V_{OUT5} at different pressure levels.

	Normal	First Level	Second Level	Third Level
$V_{OUT5\ PEAK}$	5.0V	6.5V	9.0V	13.0V

Table 2 – The Output Peak Values of the Band Pass Filter

5. The Active Full Wave Rectifier or The Absolute Value Circuit

The next stage of the project is the Active Full Wave Rectifier circuit. This circuit is also known as the Absolute Value circuit. The circuit doubles the operating frequency of the system to enhance the performance of the Peak Detector circuit in the system.

Figure 12 shows the schematic diagram of the Absolute Value circuit. In the circuit, $R_{20} = R_{21} = R_{22} = R_{24}$. In order for the circuit to function properly, the resistor R_{23} must be half of the other resistors. Therefore, a 10kΩ–22 turn rheostat is used to accomplish this task.

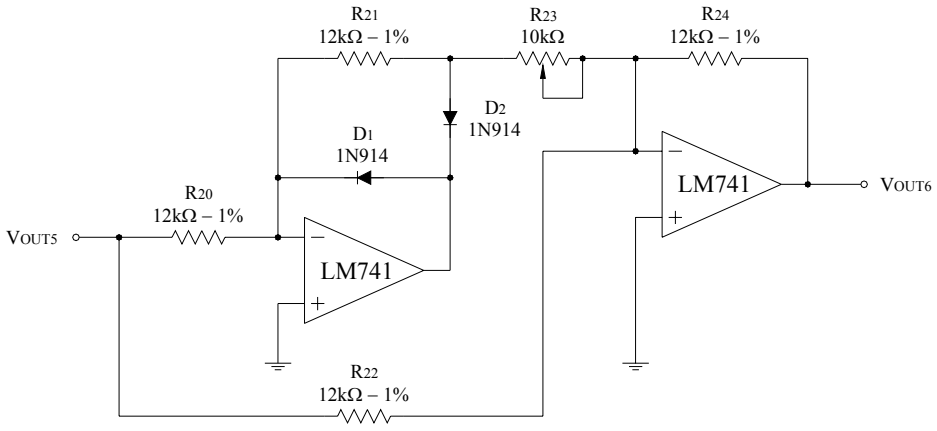

Figure 12 – The Absolute Value Circuit

Figure 13 below shows the output waveform of the Absolute Value circuit after the rheostat R_{23} is properly set.

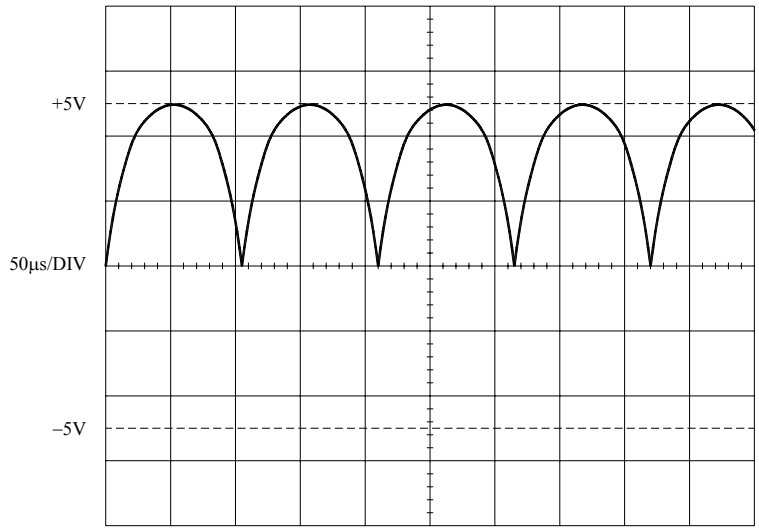

Figure 13 – The Output Waveform Under Normal Condition

Table 3 below shows the peak values of V_{OUT6} at different pressure levels.

	Normal	First Level	Second Level	Third Level
$V_{OUT6\ PEAK}$	5.0V	6.5V	9.0V	13.0V

Table 3 – The Output Peak Values of the Absolute Value Circuit

The full-wave rectified signal is then converted into a DC voltage by the Peak Detector circuit.

6. The Active Peak Detector Circuit

The schematic diagram of the Active Peak Detector circuit is in Figure 14 below.

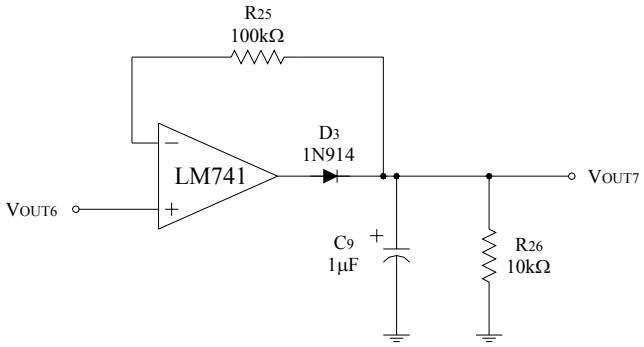

Figure 14 – The Active Peak Detector Circuit

The output signal V_{OUT7} is a DC voltage that has a small ripple voltage riding on it. Under normal condition, this peak-to-peak ripple voltage is:

$$V_{RIPPLE} = \frac{\frac{5V}{10k\Omega}}{(9.64kHz)(1\mu F)} = 51.87mV$$

Figure 15 on the next page shows the ripple voltage (with the AC input selector mode of the oscilloscope) of V_{OUT7}.

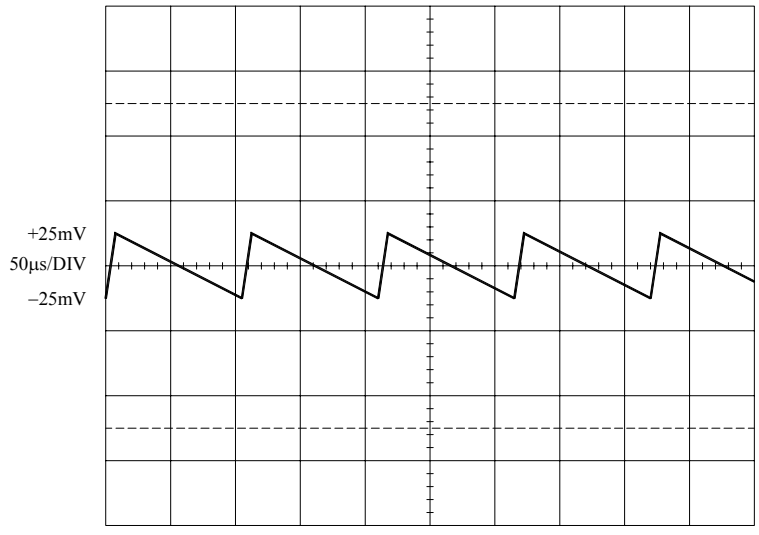

Figure 15 – The Ripple Voltage of V_{OUT7}

Figure 16 below shows the output of the Peak Detector circuit V_{OUT7} under normal condition, the first, second, and third levels of pressure.

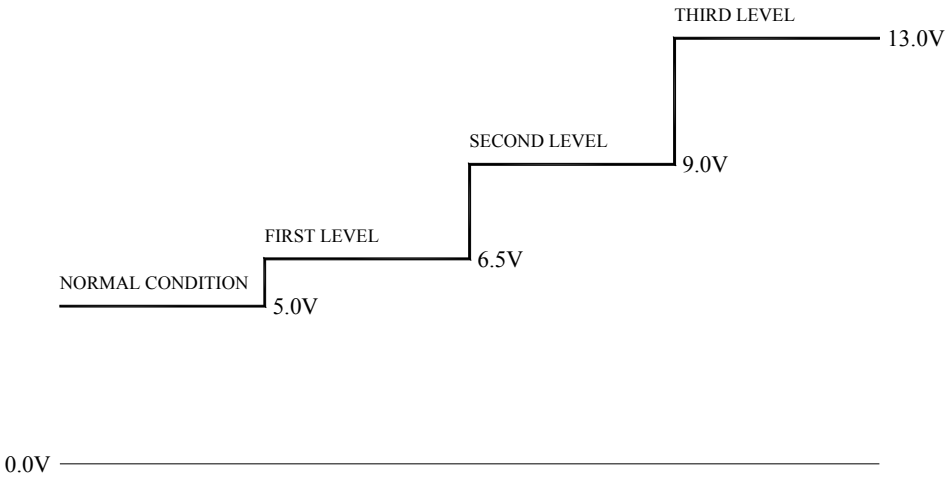

Figure 16 – V_{OUT7} Under Different Conditions

This output is used as the inputs of the three Voltage Comparator circuits.

7. The Voltage Comparators

The next stage of the project consists of three Voltage Comparator circuits. The schematic diagram of this stage is in Figure 17 below.

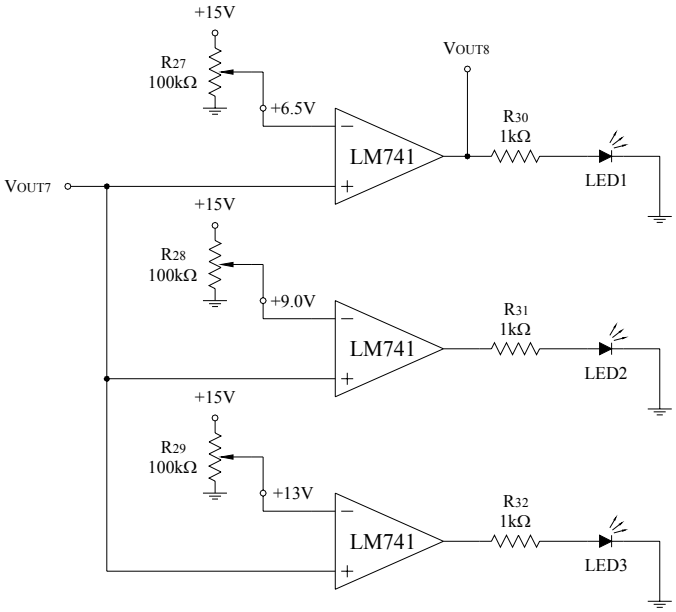

Figure 17 – The Voltage Comparator Circuits

In these circuits, the potentiometers R_{27}, R_{28}, and R_{29} are used to set the reference voltages for the Voltage Comparators. The settings are 6.5V, 9.0V, and 13.0V respectively.

Under normal condition, all three LED's are off. When the pressure reaches the first level, the light-emitting-diode LED1 is on. When the pressure reaches the second level, the light-emitting-diodes LED1 and LED2 are on. When the pressure reaches the third level, all three light-emitting-diodes are on.

This stage is the end of the analog section of the design.

C. The Digital Section of the Project

1. The Transistor Driver and the One-Shot Circuit

Since the Counters in the later part of the design require an active LO signal to function, a transistor driver is used to achieve this objective. In addition, a Monostable Multivibrator (One-Shot) circuit is also used to reset the Counters. The schematic diagram of this section is in Figure 18 below.

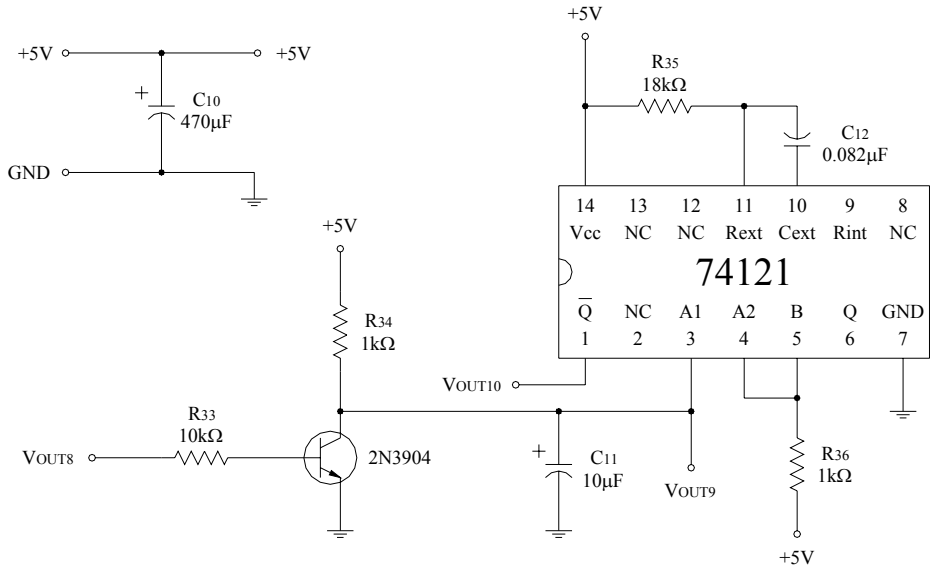

Figure 18 – The Transistor Driver and the One-Shot Circuits

In the circuit, another 470µF capacitor C_{10} is used to filter the +5VDC power supply.

The design of the One-Shot circuit is based on the Function Table in Figure 19 on the next page.

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

Figure 19 – The Function Table of the 74121

The output pulse width of the 74121 is:

$$PULSE\_WIDTH = 0.7R_{35}C_{12} = 0.7(18k\Omega)(0.082\mu F) = 10.3ms$$

The above pulse is used to reset the Counters.

The timing diagram of the circuit is in Figure 20 below.

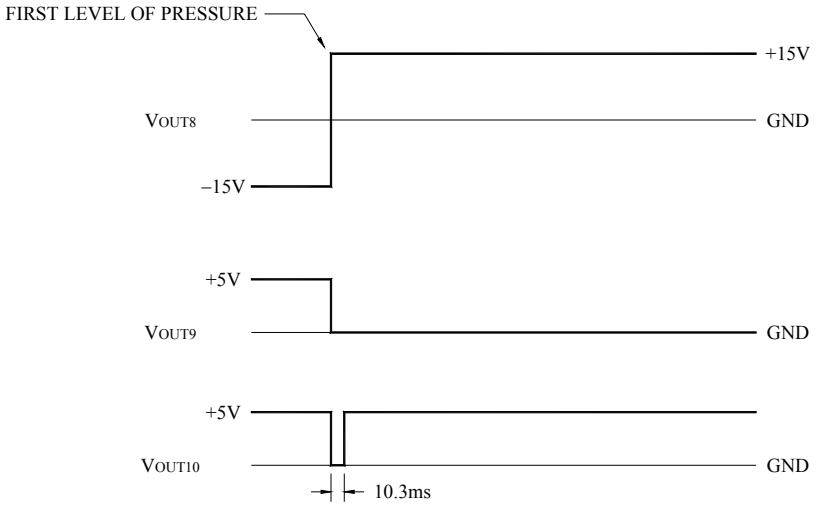

Figure 20 – The Timing Diagram of the Outputs

The output voltage V_{OUT9} enables the Counters and the output voltage V_{OUT10} resets the Counters.

2. The Clock Circuit

The next part of the digital section is the Clock circuit that generates a 10Hz square wave signal for the Counters. The circuit is a 555 Timer in its astable mode.

The schematic diagram of the Timer is in Figure 21 on the next page.

The output frequency of the Timer is:

$$f = \frac{1.44}{(R_{37} + 2R_{38})C_{13}} = \frac{1.44}{[1k\Omega + 2(330k\Omega)](0.22\mu F)} = 9.9Hz$$

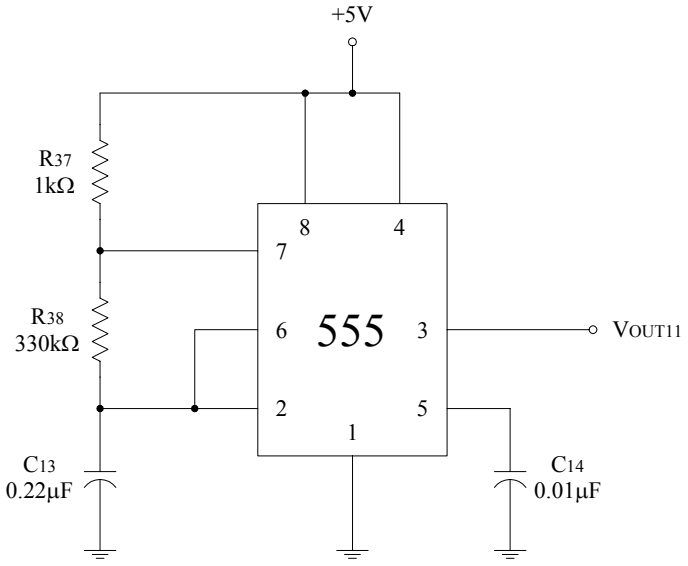

Figure 21 – The 555 Timer Circuit

3. The Counter and Driver Circuits

The schematic diagram of the last part of the design is in Figure 22 below.

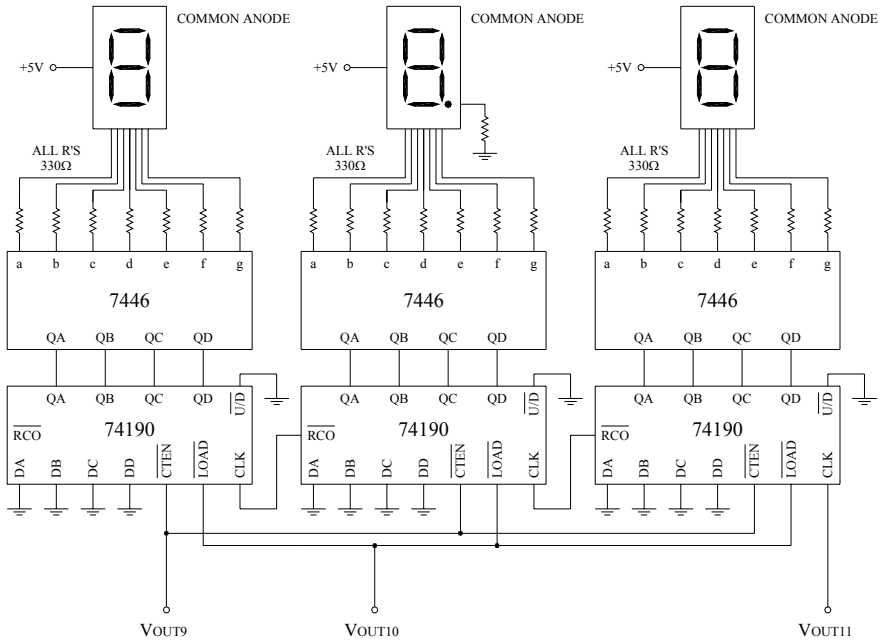

Figure 22 – The Counter and Driver Circuits

When the pressure reaches its first level, the voltage V_{OUT9} enables the Counters and the voltage V_{OUT10} resets the display to 00.0 in about 10ms. After that, the display shows the time the pressure is present to 1/10 of a second. After the pressure is released, the display freezes to show the total time the pressure was at the switch. If the switch is pressed again to the first level of pressure, the three-digit display resets to 00.0 and then starts showing the time as before.

D. Conclusion

The project produces indicators for the relative position between the top and the bottom plates of the variable capacitor. Three light-emitting-diodes show that the gap between the two plates is being closed. A three-digit display shows the total time the gap is at a preset level.

The project consists of different analog and digital circuits that the students have learned during the first three semesters in the Electrical and Computer Engineering Technology Program of Purdue University. This design gives the students an opportunity to put into practice the theories and applications they possess. It also enhances their troubleshooting skills.

This project concept has been used in ECET 297 and it predecessor course ECET 296 for the past six years. Each year the project has changed and grown in complexity. The faculty members of the ECET department in New Albany have used the results of the project to gauge overall academic success of their program. Since the project has grown each year in both size and complexity and nearly all of the students have succeeded each of the six years, the faculty believes that this is an indication of increasing strength in the program.

Bibliography

1. Boylestad, R. L. (1995). Introductory circuit analysis (6th ed.). Ohio: Merrill Publishing.
2. Budak, A. (1974). Passive and active network analysis and synthesis. Boston: Houghton Mifflin.
3. Malvino, A. P. (1999). Electronic Principles (6th ed.). Ohio: Glencoe/McGraw-Hill.

NGHIA T. LE

Nghia T. Le is an Assistant Professor of Electrical Engineering Technology of Purdue University. He teaches at Purdue University, School of Technology at New Albany, Indiana. He earned his B. S. and M. E. E. E. degrees from the University of Louisville. He specializes is instrumentation and controls. He can be reached at: nle1@purdue.edu.

TERRENCE P. O'CONNOR

Terrence P. O'Connor is an Associate Professor of Electrical Engineering Technology for Purdue University. He teaches at the New Albany site where he has taught all but one of the courses in the two year degree offered there. He is primarily interested in ELF/ULF signal detection in the area of research, but also has delved into engineering ethics. He is a graduate of Northern Arizona University where he received a B.S. in Engineering Technology. He received his Master of Science degree in Engineering Technology from West Texas State University. He can be reached at: toconnor@purdue.edu.