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Undergraduate Research Experiences Using FPGAs

Abstract

State-of-the-art Field Programmable Gate Arrays (FPGAs) can now implement designs with millions of logic gates at speeds and power dissipation that rival custom integrated circuit designs for many applications, but at a fraction of the development cost. This paper will discuss recent experiences on working with undergraduate researchers in the area of FPGA design at the University of Texas at Tyler. Criteria for the selection of appropriate research projects will be given. Issues such as methods for supervision, motivation, and funding will also be discussed. Assessment of using undergraduate student researchers in the area of FPGA design are carried out through faculty observations, generation of conference paper submissions and poster presentations, and student self-assessment through survey results.

Introduction

Modern Field Programmable Gate Arrays (FPGAs) have developed to the point where they include millions of configurable logic gates, embedded memory, and preconfigured logic blocks, such as multipliers and microprocessor cores. Engineers can use FPGAs to implement a variety of complex digital systems that rival Application Specific Integrated Circuits (ASICs) in terms of performance but at a fraction of the development costs. As a result, FPGA designs are expected to dominate the market for high performance digital systems, relegating ASICs to only the most demanding high-volume applications that justify their high development and fabrication costs[1]. Thus, it has been essential to introduce our students to the design of reconfigurable logic and to give undergraduate students the opportunity to do research in the extremely active area of FPGA design.

The University of Texas at Tyler currently has an FPGA Design class that exists as a senior elective in the electrical engineering curriculum. The class introduces the students to the process of FPGA design, from coding in the high-level descriptor language VHDL to using the tools to synthesize and debug a design. However, actual research in this area had been restricted to graduate students. This paper describes an effort that began two summers ago to involve undergraduate students in FPGA research at our institution. Other institutions have reported the benefits of introducing FPGA design projects into the curriculum[2] and producing research where the components of FPGA-based projects were completed by undergraduates[3]. The experiences in this paper are unique in several ways. First, the undergraduates are introduced to FPGAs in a summer seminar session before they have been formally introduced to FPGAs in a course. Second, the research is carried out throughout the academic year with appropriate motivation used throughout the process. Third, some of the research that was produced mainly by the efforts of the undergraduate students over a one year span resulted in conference presentations.

This paper is outlined as follows. The context and history will be described first from the initiation of this research program with one undergraduate student in the summer of 2010. Next, the effort with three more undergraduate students this past summer will be described in detail, including a discussion of the training method, supervision, and selection of the research projects.

The ongoing research efforts this past fall will also be covered. This will be followed by a discussion and evaluation of results with guidelines for keys to success for undergraduate research. Finally, some conclusions and future plans will be discussed.

Background and Initiation of Undergraduate Research

This section provides some background on the FPGA Design class offered at our institution and a brief history of how undergraduate research in FPGA design was initiated.

The FPGA Design class introduces the student to the concepts of reconfigurable logic design, including how to write VHDL code to synthesize basic digital logic designs, such as counters and adders, as well as how to use the tools for simulation and debug. Our laboratory is equipped with FPGA development boards from Xilinx. The students learn how to use the associated design software from Xilinx, which includes the ChipScope virtual logic analyzer, the PlanAhead tool, and the ISIM simulator[4]. Some unique features of this course include a discussion of the relevant VLSI design issues, testing FPGAs using high speed logic analyzers, and design with soft processor cores. An understanding of the VLSI design issues gives the students insight into the challenges of FPGA design, such as wire delay, optimum number of lookup-table (LUT) inputs, and designing programmable interconnect and input/output interfaces. Such insight is essential for designing high-performance circuits with FPGAs. Our lab is equipped with several high speed logic analyzers, and the students get first-hand exposure to how this equipment is used to characterize and debug an FPGA implementation. Design with soft processor cores is emerging as an important area in FPGA design, especially the implementation of multiprocessor systems using reconfigurable logic[5,6]. Three laboratory sessions are devoted to designing with an 8-bit microcontroller synthesized on an FPGA.

Up to two years ago, undergraduates were not involved in research using FPGAs since they typically took the FPGA Design class during their senior year. In the summer of 2010, the author decided to do research in this area with one student who had just finished his junior year but had not taken the FPGA class. (For convenience, students will be identified in this paper by their initials.) The student (CM) was funded by the NSF Louis Stokes Alliance for Minority Participation (LSAMP) program. Having taken the required classes in Digital Systems and Microprocessor Design, CM was able to learn how to synthesize designs on an FPGA using VHDL by working through some of the tutorials with the help of a graduate student. An MSEE thesis had just been completed by this graduate student on the design and characterization of parallel-prefix adders implemented on FPGAs. The undergraduate student CM was assigned the project of developing the testing methodology for these adders using our high-speed logic analyzer. This involved implementing an on-chip pattern generator using the Block RAM on the FPGA, developing a suitable test pattern that exercised all the internal nodes, and having a method to cancel out wire delay. The author met with the student several times a week to supervise this project but in large part the student was able to work independently. Based on the undergraduate student's testing and the work of the graduate student, a conference paper was presented in March 2011[7]. The key to success was finding a motivated student able to get up to speed quickly on FPGA design and assigning a project within an existing framework created by the graduate student. The availability of the graduate student during the first six weeks of the summer to assist the undergraduate student was also helpful.

In the Fall 2010, another undergraduate student (MC) expressed interest in FPGAs through learning about CM's work. An independent study for the Fall 2010 semester was set up for MC to learn how to design with FPGAs and an appropriate research project was assigned to him. The criteria for an appropriate project for an undergraduate is one that is manageable and yet is challenging and has potential impact. As has been noted by others, work that is publishable provides some extra motivation for the student.[8] A topic in cellular computation that meets these criteria was assigned to the undergraduate student. Cellular computation, where small autonomous cells communicate with just their neighbors, has been touted as the future of computing using nanotechnology due to their simple architecture and their ability to efficiently handle complex calculations through massive parallelism[9]. Cellular automata represent a form of cellular computation. Because of their regular structure and local interconnect requirements, they can be efficiently implemented on FPGAs. Figure 1 depicts a one-dimensional cellular automata where the state of each cell is determined by a rule which is a function of a cell's current state and the state of its two immediate neighbors. This nearest neighbor cellular automata was studied extensively by Wolfram, who suggested certain rules could form the basis for implementing efficient pseudo random number generators (PRNGs).[10]

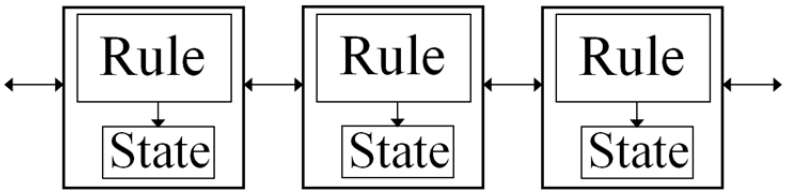

Figure 1. A one dimensional nearest neighbor cellular automata (CA).

Cellular automata are conceptually not that difficult to understand or implement on an FPGA. Previous research has focused on simulation or developing custom chip designs to implement cellular automata. Hence, porting a cellular automata design to an FPGA makes for a suitable undergraduate project and could result in publishable research. The basis of MC's research was a recent paper that focused on an integrated circuit approach to implementing a self-programmed cellular automata PRNG[11]. The student's research involved translating this design to an FPGA implementation and evaluating its effectiveness. The student MC was able to obtain funding from our institution's Office of Sponsored Research (OSR) in the Spring 2011 semester to work on this project. A simulation program was written in C to generate the large quantities of numbers needed to test the quality of the random numbers and an FPGA design was implemented. The student presented his work at a poster competition sponsored by the OSR in April 2011.

Based on this success, four undergraduate students were involved in research this past summer (2011). The remainder of this paper will focus on these FPGA projects and the associated lessons learned for successful supervision of undergraduate research.

Research During the Summer

Important issues, such as supervision, training, funding, and selection of projects from this past summer will be detailed in this section. Regarding supervision, the author scheduled meetings twice per week with the students during the summer. On Tuesdays, group meeting were scheduled with the undergraduates and the two graduate students who were assisting with the research. On Thursdays, the author met individually with the students in the lab to assist them with their research projects. As none of the undergraduate students had taken the FPGA Design class yet, it was necessary first to teach them how to design with FPGAs. The group meetings were initially dedicated to going over the lecture notes and the laboratory assignments from the FPGA class. The students were required to do some learning independently and then work on the FPGA tutorials in the lab. What was helpful was having the two graduate students working in the lab who were willing to help tutor and assist the students through this learning phase. The author's observation was that the students were able to grasp the basics of VHDL coding after three weeks of training. At this point, they were assigned research projects to work on.

Table 1 summarizes the students involved and their assigned projects. In this case, the goal was to assign the undergraduate students a meaningful but manageable project keeping in mind that the students had minimal experience in designing with FPGAs at this point. Manageable frameworks that allowed them to make significant progress during the summer were ensured by assigning projects that had been developed somewhat by previous students (cellular automata and adder designs) or discussed in the FPGA class (soft processor cores). The student CM was the one who worked in the summer of 2010 with the author. He was actually working with the author on a research project not related to FPGAs (Carbon Nanotube Transistor amplifier) in the summer of 2011, but was present in the meetings and lab to help mentor the other three with their FPGA projects.

Table 1. Student Research Projects for Summer 2011

Student	Project
1. Senior (CM)	Carbon Nanotube Transistor amplifier design
2. Junior (JC)	Cellular automata random number generator
3. Sophomore (YG)	C program for generating wide-bit tree adder designs
4. Sophomore (IO)	Soft processor cores using the MicroBlaze processor

The junior student (JC) was able to build upon the cellular automata work that was started in Fall 2010. Existing C code for simulating cellular automata had been written and methods for evaluating the quality of random numbers had been established through the use of the DIEHARD program[12]. This student's project was to combine two methods for generating random numbers: cellular automata and linear feedback shift registers (LFSR). This method had been proposed previously in the literature[13], but had not been investigated using FPGAs. The interesting approach in the context of FPGAs is that the LFSR component can efficiently be generated using the FPGA's lookup tables since they can also function as shift registers[14]. Thus, this study endeavors to understand the impact of using larger LFSR combined with smaller CA's on the

quality of random numbers generated. A typical configuration consisting of a 37 bit LFSR and a 16 bit CA that was investigated is shown in the figure below. The fact that the Look-up Tables (LUTs) can be converted into shift registers allows the LFSR to be efficiently implemented on an FPGA. In this example, the two blocks labeled SR16 form a pair of 16-bit shift registers.

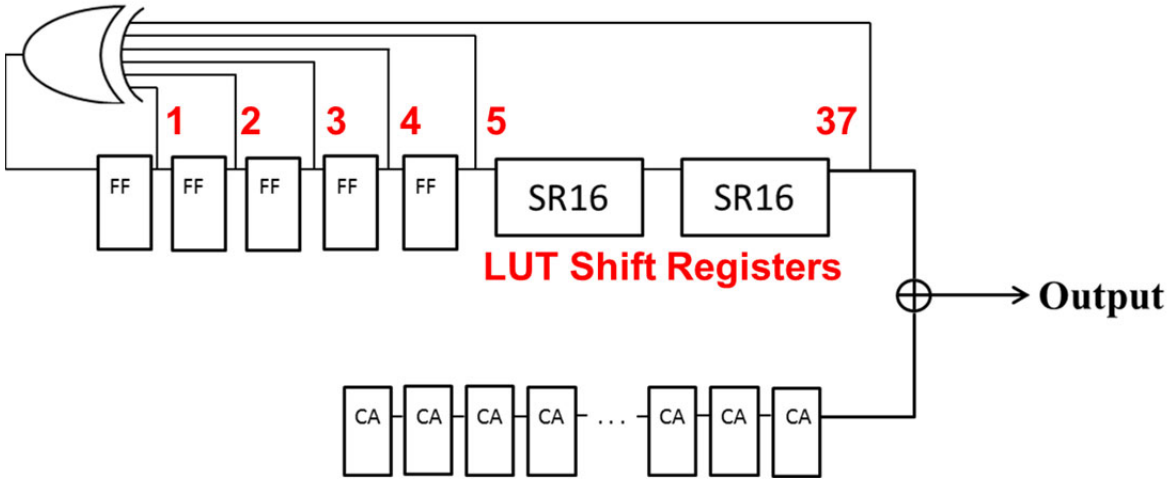

Figure 2. A PRNG constructed from a hybrid combination of a 16-bit cellular automata (CA) and a 37-bit LFSR. The taps of the LFSR are numbered.

The wide-bit tree adder design project tasked the undergraduate with writing C code to automatically generate VHDL code to allow synthesis of adders with 128 bits and wider. This built upon a previous study of wide-bit parallel prefix adders, where the delay characteristics of various adder topologies were studied on FPGAs[7]. Thus, student YG was able to study the existing VHDL code to be able to understand how the adder is structured and coded. This was a good project for this student since she is doing a minor in computer science. The soft processor core project using the MicroBlaze processor was assigned to a student who is interested in microprocessor design. This basically extended the work that was carried out in the FPGA class where the students are exposed to a simpler 8-bit soft processor core on the FPGAs. The MicroBlaze processor is Xilinx's IP core 32-bit RISC microprocessor. The Xilinx design software provides resources for creating the hardware on the FPGA for communicating between processors and several researchers have already published papers discussing the use of the MicroBlaze processor as the basis for a multiprocessor design on FPGAs[5,6]. This student was tasked with investigating these approaches and to try implementing them on our Xilinx Virtex 5 FPGA development boards.

In addition to learning how to synthesize designs on the FPGA, the students also gained experience using the high-speed logic analyzer in our lab. The figure below illustrates the testing of the cellular automata design using a Tektronix TLA7012 logic analyzer. The signals are taken off the board through a low-capacitance soft-touch landingpad and the 20 ps resolution of the logic analyzer allows delay information to be directly measured.

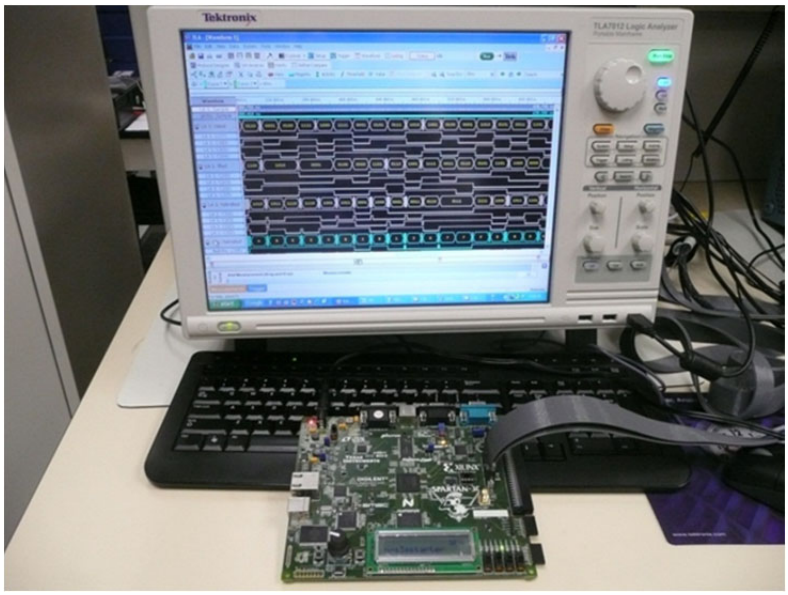

Figure 3. Test setup showing the Spartan 3E FPGA development board connected to a Tektronix TLA 7012 logic analyzer.

Research During the Fall Semester

The key challenges involved in supervising the undergraduate students this past fall semester are discussed in this section. This includes keeping the students motivated and the importance of time management (from both the student and faculty perspective) while classes are scheduled.

Methods for motivation include group activities and working on a conference publication. To encourage the students to work together and also expose other students to their research, a student organization was officially formed with the core group of students serving in leadership roles. We decided to highlight the research into cellular automata, since it is the most interesting from both a technological and philosophical point of view. The club was called the "Cellular Matrix" as the main goal was to study cellular automata in Wolfram's book *A New Kind of Science*[10]. The interesting philosophical issues are associated with Wolfram's conjecture that the universe should be understood in terms of simple computer programs. For the statement of purpose for our organization, we wrote:

> To discuss and promote interest in all things related to Cellular Automata. This semester we'll read Stephen Wolfram's "A New Kind of Science" and discuss its scientific and philosophical implications (e.g., is the universe a giant cellular automata and does it explain quantum mechanical concepts such as action at a distance?). Some other activities include writing Cellular Automata code for the Game of Life and the Prisoner's Dilemma. If time permits, a study of Additive Cellular Automata will be undertaken.

Some activities such as building Game of Life electronic kits and discussing these philosophical issues inspired the students to think about issues relevant to their research while providing a fun and team-oriented atmosphere. This sort of motivation is especially important when there is not a

lot of funding to support undergraduate research. (Of the undergraduate students, only JC was supported by the continuation of the LSAMP funding.) The weekly meeting also provided some opportunity to discuss the research as well.

While the club was important, the prime motivator was writing a conference paper. Impressing upon the students the importance of having a conference paper on their CV as a way to stand out when looking for a job or applying for graduate school seemed to motivate them to "go the extra mile" in getting some useful test results. Indeed, the students JC, MC, and CM spent several late Friday evenings gathering test results for the papers they were working on. An assessment of what research was accomplished and the papers that were written is discussed in the next section.

In terms of time management, establishing some set times to meet with the students is essential. For the most part, the author met the students as a group, once per week, in order to effectively supervise the students without expending an excessive amount of time. As in the summer, the assistance of graduate students in this endeavor is very valuable for ensuring progress is made without requiring too much faculty intervention.

Assessment

An assessment of the effectiveness of utilizing undergraduate students in research are discussed in this section. Methods for assessment include faculty observation, resulting conference and poster presentations, and student self-assessment through a survey given at the end of the summer session.

Faculty observation: The experiences of the past two years have impressed upon the author the effectiveness of utilizing undergraduate researchers under the right conditions. While graduate students have formal research objectives through their thesis requirements, undergraduates do not have this as a driving force to do research. Thus, finding motivated students and challenging them through meaningful but manageable projects is one important consideration. The author recruited the two sophomore students to do research by interviewing the best students in the department's Microprocessors class. When given a framework to do research within their educational background, the students were able to contribute to research that is publishable at a regional IEEE conference. As noted previously, the assistance of graduate students is also important from a time management point of view. The project should complement the graduate student work, so that the graduate students are willing to give a hand. Institutional support is also important in terms of providing resources and funding for the students. For the summer research, the students were funded through various means: NSF LSAMP (JC), internal grant (CM), and use of start-up funding (YG and IO).

Conference papers: Based on the research from this past summer 2011, two papers were presented at a regional IEEE conference in March. The paper entitled "Random Number Generators using Cellular Automata Implemented on FPGAs"[15] has demonstrated some novel configurations within the context of an FPGA implementation for generating high quality random numbers. This paper was solely due to the research of the undergraduate students and they had a major role in the actual writing of the paper, which is unusual for students at this level.[8] The second paper entitled "A Fault Tolerant Parallel-Prefix Adder for VLSI and FPGA

Design"[16] was written by graduate students but the work of the undergraduate YG contributed to the design of the wide-bit tree adders that formed the foundation of the design. An example of one of the fault tolerant adder designs from this paper is illustrated in Figure 4. In this example, a carry-tree design known as a Kogge-Stone adder was implemented on an FPGA. This particular design is a sparse Kogge-Stone adder, which contains a mixture of a carry-tree terminated with a set of ripple carry adders (RCAs). The length of the RCAs determines the degree of scarcity in the carry-tree. The red colored blocks highlight the additional fault tolerant hardware. Two additional RCAs are added (called TestRC) to provide fault detection and correction for the RCAs designated as RC0 to RC3. Each of the RCAs is tested once every four clock cycles by comparing its output with the two Test RCs.

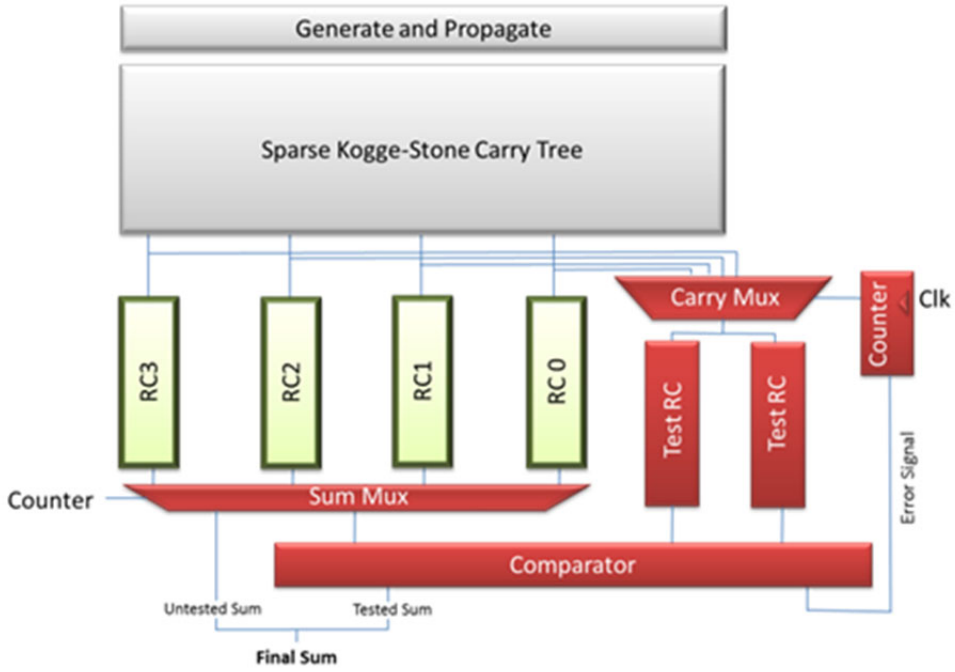

Figure 4. Block diagram of Fault Tolerant Sparse Kogge-Stone Adder.

In addition, student JC achieved good scores when he presented his research at a regional LSAMP poster competition in September 2011. He has continued to work on the LFSR and CA random number generator under LSAMP funding during the fall and spring semesters. Another conference paper is being submitted based upon further developments in his research.[17]

Survey results: The students were asked two questions on a survey given to them at the end of the summer of 2011. When asked what they liked most about their summer research experience, two students noted working with a faculty member on a project, one noted working with other students. Positive comments were also made regarding working on real world applications and being able to get a FPGA design to function. When asked what they would do to improve their summer research experience, two students gave responses. One noted that more one-on-one time with the faculty was needed to make substantial progress on the research, and another noted that more (paid) hours per week was desirable. The students were also asked to rate four statements on a 1 to 5 scale as summarized in the table below.

Table 2. Student Attitudes towards Research during Summer 2011
(*Scale*: 1= Strongly Disagree, 2= Disagree, 3 = Neutral, 4= Agree, 5 = Strongly Agree)

Question	Rating
1. The weekly group meetings were helpful for learning VHDL and the context of my research assignment using FPGAs.	4.75
2. It was helpful to have a graduate student work with me on my research	4.75
3. Given the amount of hours that I was paid for research, I feel that I accomplished a meaningful amount of research this summer	4
4. At the conclusion of my summer research experience, I was more inclined to consider graduate school in electrical engineering.	4.75

Overall, it appears the students were satisfied with the way they were supervised during the summer months. The lower rating for the third statement is likely due to the fact that the available funding allowed the two sophomore students to be paid for only ten hours per week during the summer months. It is gratifying to see that the summer research experience had a positive impact on the students' plans for graduate school as reflected in the response to the fourth statement.

Summary and Conclusions

Several important lessons learned for enabling successful undergraduate student research in FPGAs are now summarized. First, while rather obvious, it is worth stating again, the importance of finding the right quality of student. Students who are motivated and especially those who are pondering graduate school are key.[8,18] All five of the students represented in this paper are considering graduate school or have already applied. (One of them, CM, has already started his MSEE degree at our institution.) Ideally, the students need to be able to work independently for stretches of time, take instruction well, and be able to work and help others. The latter point is important since group synergy is helpful as one student noted in the survey. Second, one should take advantage of funding sources available for undergraduates. Our institution has funding from NSF's LSAMP program and our OSR sponsors student research through poster competitions. The author found it works best to identify students that he wants to work with and encourage these students to apply for this funding. Based on this success, the author is also including some funding for undergraduates in all his future research proposals. Third, assigning students manageable projects within an existing framework is another important key to success. This should build upon another student's work (e.g., testing the tree adders) or be something conceptionally not too difficult but ideally have significant interest and impact (e.g., the use of cellular automata to implement PRNGs). Fourth, finding some graduate students who are willingly to work with the undergraduate students is also important. One way to ensure this is to assign projects that complement the thesis work being carried out by a graduate student. Lastly, the possibility of generating a conference paper through the research is a very strong motivator. Undergraduates students generally will require coaching on writing the paper, but by involving the students in both the research and writing of the paper, they have a sense of ownership in the

process.[8] This encouraged the students to give an extra effort as noted by the several Friday evenings they were observed to be working in our FPGA lab on their research projects.

In sum, as FPGAs become capable of implementing more complex designs, they will be an increased source of research activity for applications that were once the sole domain of ASICs. While undergraduate students generally require more supervision than graduate students, under the right circumstances outlined in this paper, it is found that undergraduate students can make a meaningful contribution in this area. Moving forward, the author plans to look for more fundable projects for undergraduates in the active area of FPGA research.

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