Undergraduate Research in Nanotechnology Circuit Design

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Abstract

Undergraduate research in the area of nanotechnology circuit design is described. Two undergraduate students worked with electrical engineering graduate students and a faculty member on projects related to designing nanoscale logic gates and circuits using single electron transistors and by using quantum cells. In this paper, the undergraduate research projects carried out by the two REU students are summarized

1. Introduction

Active research experience is one of the most effective techniques for training and motivating undergraduate students for careers in science and engineering. National Science Foundation (NSF) recognizes this and supports undergraduate research under "Research Experiences for Undergraduates (REU) Supplements" program where it encourages principal investigators of NSF-funded research grants to include one or two undergraduate students in their existing projects. This paper summarizes the experiences of two such REU students (CR, DG) who worked on research projects in nanotechnology circuit design under the supervision of graduate students (AV and others) and faculty (AG).

The semiconductor industry has been constantly working on shrinking the size of the MOSFET to increase the device density and data transfer rate for the integrated circuit. The current trend of MOSFET scaling may fall apart when the transistor sizes are shrunk to a few nanometers. At the nanometer scale, quantum behaviors come into effect and cause undesirable effects such as subthreshold leakage, gate oxide leakage, increased transistor parameter variability and interconnect density and performance. In order to overcome these hurdles for producing high density chips with low power consumption, some of the devices in the nanometer scale that are being studied by research groups as possible replacements for MOSFETs include carbon nanotube transistors, nanowire FETs, single electron transistors (SET) [1-11] and quantum dots [12-14].

One of the REU students (CR) worked on a project whose goal was to extend the widely used MOSFET-based CMOS technology to designing CMOS logic gates using the single electron transistor technology. First, she learnt the physics of these devices and their

current-voltage characteristics using a nanostructure simulator called SIMON [11]. Then she worked towards finding the optimum values of the SET design parameters for the development of practical logic gates and circuits. The other REU student (DG) has developed a first level quantum cellular automata simulator called QCAS which has been used to simulate various logic gates built by using quantum dots and quantum cells. QCAS has been used to simulate circuit components such as a quantum wire, a wire bend, crossing wires, a majority gate and more complex logic gates [12]. While the design and simulations of simple logic gates proves the amazing potentials of these two nanodevice technologies, it is important to implement more complex logic operations to make use of these devices in practical circuits working under various operating conditions.

2. Designing Nanotechnology Circuits Using the Single Electron Technology

Single Electron Transistors are the wave of the future for electronic applications around the world [1-10]. Their performance in everyday life, however, depends on their operation under practical conditions. Overcoming this obstacle seems to be easier said than done. By using SIMON, we were able to simulate Single-Electron Devices in order to realize their performance under different conditions. With the help of SIMON, finding these optimal parameters has been one of the goals of this project.

The basic layout of an SET is a small conducting island coupled to source and drain leads by tunnel junctions that are capacitively coupled to one or more gates. Single Electron movement deals with a small amount of excess electrons on islands changing their distribution on the islands over time. The charges in single-electron devices are transported in a quantized way rather than continuously which implies that SETs are very sensitive to charge. Poorly permeable tunneling barriers separate the islands that make up an SET. A charge is stored on each island and one electron can be transported from one island to the other. Initially uncharged, a voltage is applied that makes the charge carriers gather at the tunnel junction. After a period of time, a single electron will move from one island to the other. The presence of this one electron on one island and its absence on the other is significant due to the already miniscule charges held by the islands.

2.1 Single Electron Transistor Simulations

A basic Single-Electron Transistor from SIMON is shown in Fig. 1. The voltage of the island is a function of the number of electrons on the island and is given by

$$V(n) = (-n*e + Q_0 + C_1*V_1 + C_2*V_2 + C_{g1}*V_{g1} + C_{g2}*V_{g2}) / C_?$$

where n is the number of electrons, e is the positive elementary charge and $C_?$ is the total capacitance of the island = $C_1 + C_2 + C_{g1} + C_{g2} + C_0$.

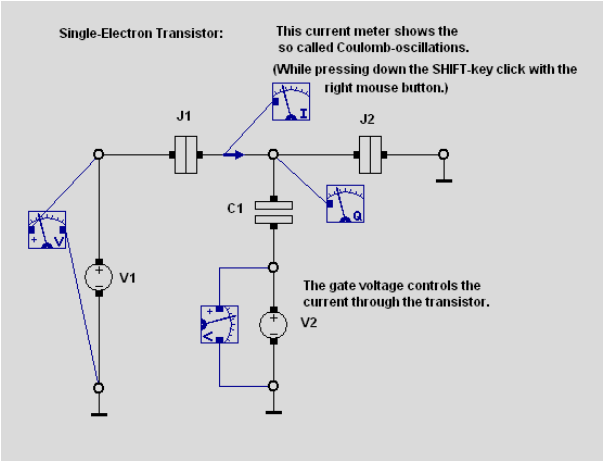

Fig. 1: Schematic diagram of an SET from SIMON [11]

In order to determine the effects of temperature and capacitance values on the operation of the transistor, they were altered separately for each test simulation. In the first set of simulations, temperature was changed and its effects were observed, while in the second set of simulations, the effects of changing capacitances at different points (C1, J1 and J2) in the device were observed. For example, simulations of an SET at temperature = 0K, 50K and 100K are shown in Figs. 2(a), 2(b) and 2(c), respectively. These results show that the temperature cannot be kept much more above around 80-100K. The step

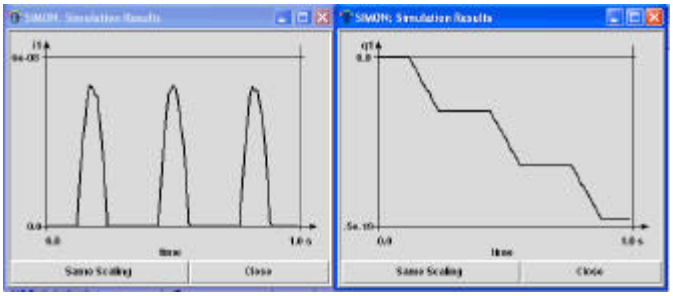

Fig. 2(a): Simulation of the initial SET with temperature = 0K and C1 = 1E-18

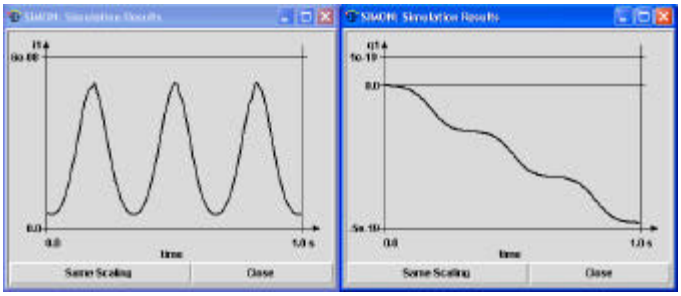

Fig. 2(b): Simulation of an SET with temperature = 50K

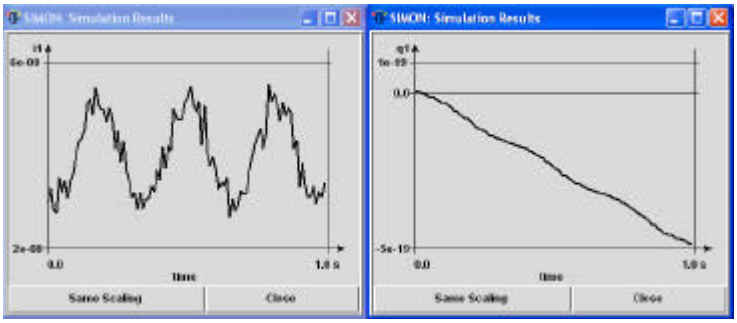

Fig. 2(c): Simulation of an SET with temperature = 100K

The possible solution to overcome this problem is to optimize capacitance values for higher temperature operation. Series of simulation by altering the capacitances at different points in the circuit was performed. For example, simulation results for an SET at a higher value of C1 are shown in Fig. 3(a) while those at higher junction capacitances are shown in Fig. 3(b). These results show that the frequency of charge

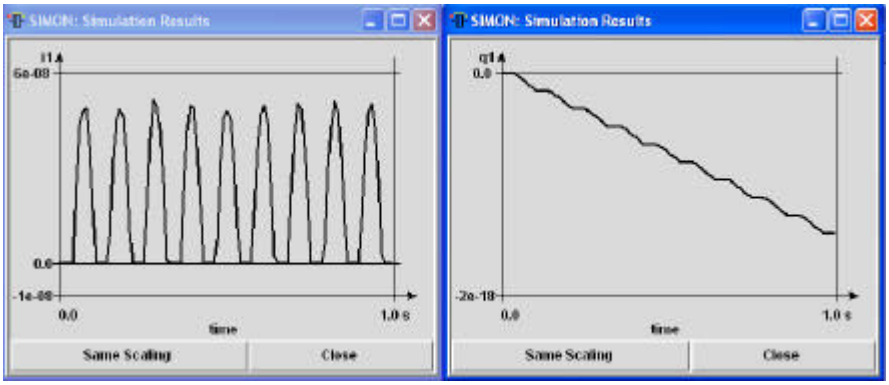

Fig. 3(a): Simulation of an SET with C1 = 3E-18 F

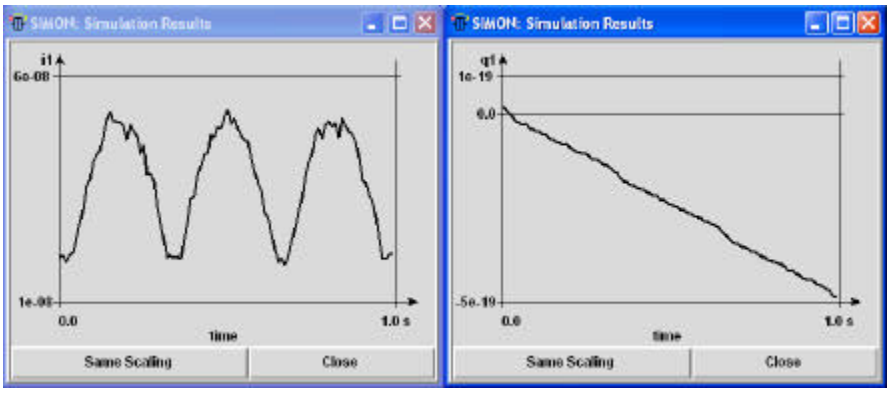

Fig. 3(b): Simulation of an SET with J1 and J2 capacitance = 4E-18 F

steps is directly proportional to this capacitance C1. Therefore this value has to be made extremely small for the device to work. As the capacitance increases, the current and charge begin to vary at a higher rate. When the capacitance of the tunnel junctions is increased, the controlled jumping of the charges becomes less and less evident.

2.2 Single-Electron Inverter Simulation

The design of an SET-based inverter and its input/output simulation results are shown in Fig. 4. The parameters were chosen in order to obtain optimal performance.

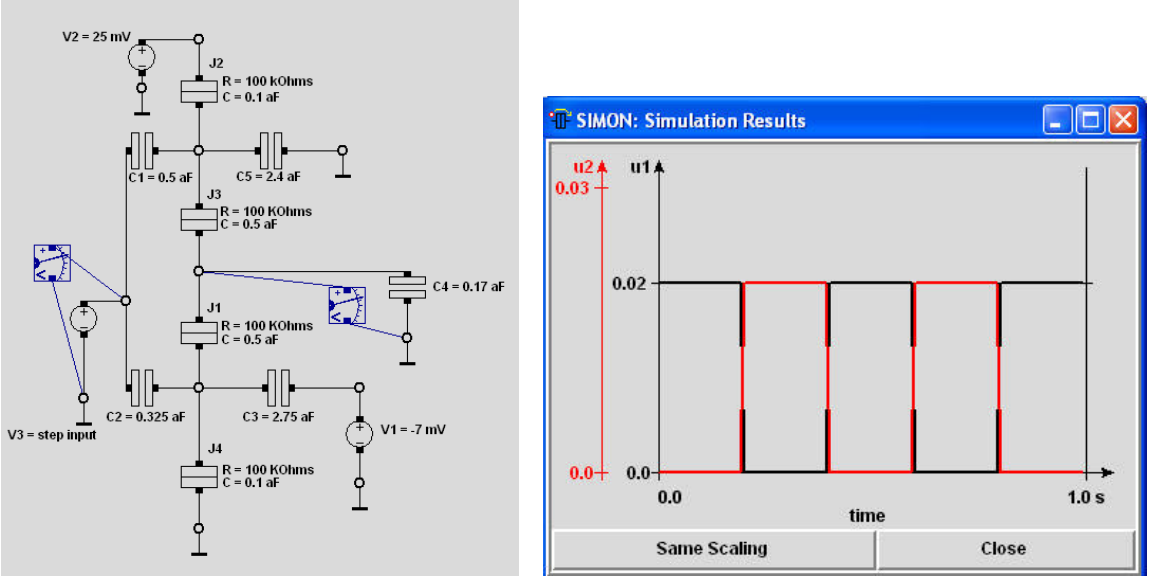

Fig. 4: SET-based inverter and its input/output plots using SIMON

2.3 Single-Electron XOR Simulation

Figure 5 shows the design and simulated operation of a 3-input XOR gate in SIMON along with the appropriate parameters in order to achieve an optimal output. This figure shows that the output signal is a lot smaller than the input signal, but its operation is correct. The output seems to be off by about a factor of ten, which shows that the SET-based gates have a poor gain.

2.4 Single-Electron XNOR Simulations

Figure 6 shows the design and operation of a 3-input XNOR gate in SIMON along with the appropriate parameters in order to achieve an optimal output. The output signals for

the XNOR gate is also much smaller than the input voltages just as seen above in the case of the XOR gate, but its operation is correct.

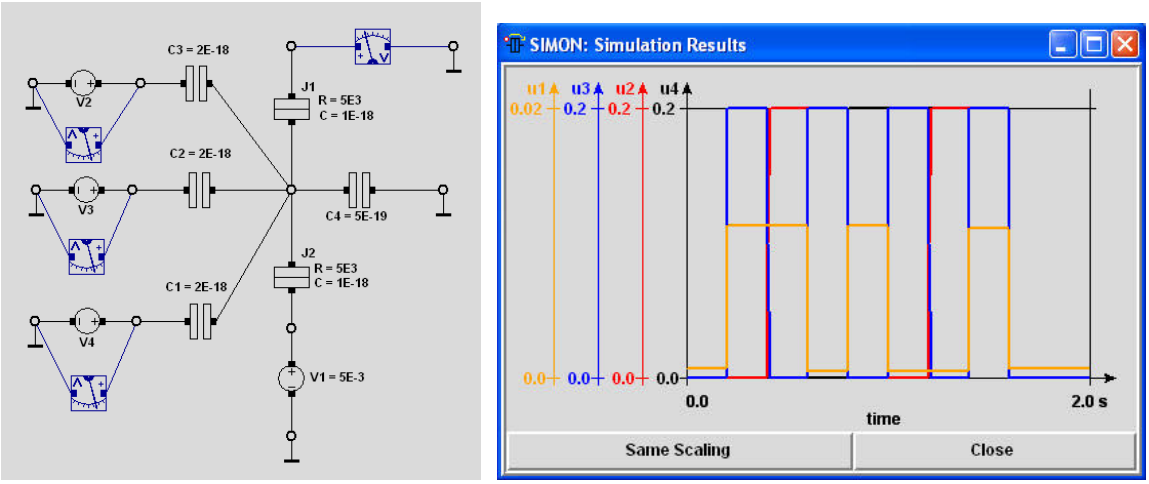

Fig. 5: SET-based 3-input XOR gate and its input/output plots using SIMON

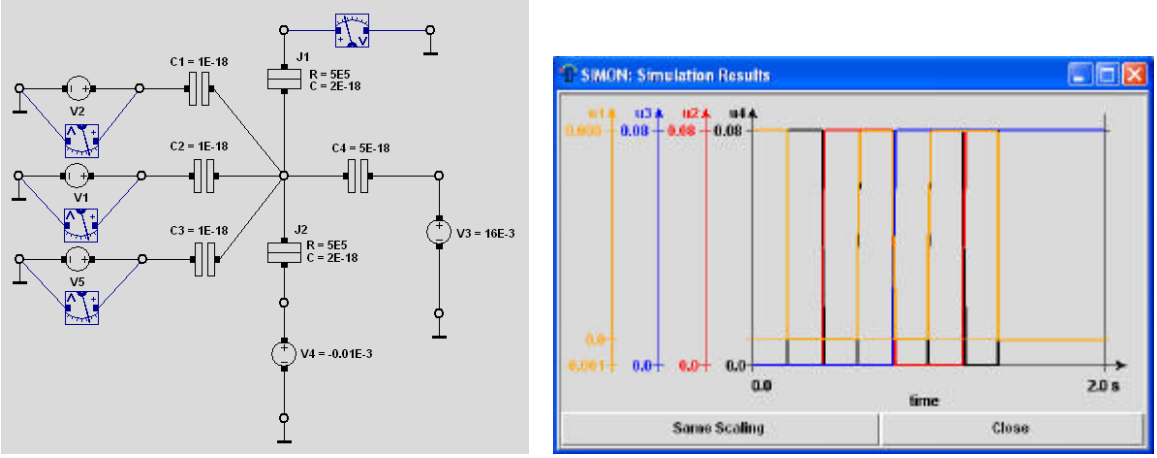

Fig. 6: SET-based 3-input XNOR gate and its input/output plots using SIMON

3. Designing Nanotechnology Circuits Using Quantum Cells

In this REU project, we have discussed the design and simulation of a Quantum Cellular Automata (QCA) memory array. The memory array was developed using the Quantum Cellular Automata Simulator (QCAS) software designed earlier [12] which uses adiabatic switching and classical physics to perform circuit simulations. Simulations were

performed on a memory array which has four lines of four bit words. Data was successfully stored and retrieved during circuit simulations.

3.1 Quantum Cellular Automata Simulator (QCAS)

Quantum cellular automaton (QCA) has promising features when compared to conventional logic circuits [13, 14]. These features include low power consumption, single layer signal crossing, and nano-scale size. A QCA circuit is comprised of cells with four (or five) dots separated by tunneling layers with two free electrons, as shown in Fig. 7. Coulomb forces tend to orient the free electrons in the diagonals, leading to two logical states. When a cell is driven by an adjacent cell, its electrons are influenced to the same logical state. The logical states in which an array of cells are in their least energy configuration is called the ground state. The QCAS program [12] colors the input cells green and colors the cells driven by other cells red. Placing quantum cells appropriately, basic circuit elements (AND, OR, NOT) can be formed. It has been shown that properly arranging these circuit elements can produce any combinatorial logic circuit.

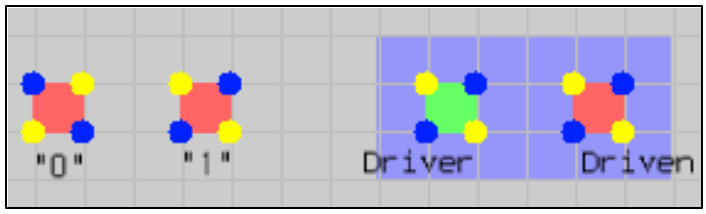

Fig. 7: Logical states and cell switching.

Adiabatic switching is a process of switching, holding and relaxing of cells using a multiphase clock. In adiabatic switching, groups of cells are influenced by a clock signal which controls the tunneling barrier between the dots. In this way, a clock signal can control when the cells switch, hold, release and relax their electron states. Adiabatic switching was used for several reasons impacting both simulation and fabrication. It has been suggested that very large arrays of cells are likely to become stuck in meta-stable state, which would produce an incorrect output or take an extraordinary amount of time to reach ground state. Adiabatic switching adds synchronization between basic circuit operations. For simulation purposes, it was found that the QCAS software runs slowly on arrays with more then 17 cells.

3.2 Design and Simulation of a QCA Memory Array

The QCA memory array was designed to contain the same features as a register memory array. For a proof of concept, an array was implemented with four lines of four bit words. The array includes a four bit input, a read/write signal, a two bit line selection, and a four bit output. The completed circuit is shown in Fig. 8. Each bit of data is stored in a small loop. Most of the circuit area is used by line selection and read/write

capabilities. Throughout the circuit, single plane signal crossing is achieved using rotated cells. AND, OR, and NOT gates are also found in the circuit's combinatorial logic. The input signals move from the top right to the remainder of the circuit. The output is at the bottom of the circuit.

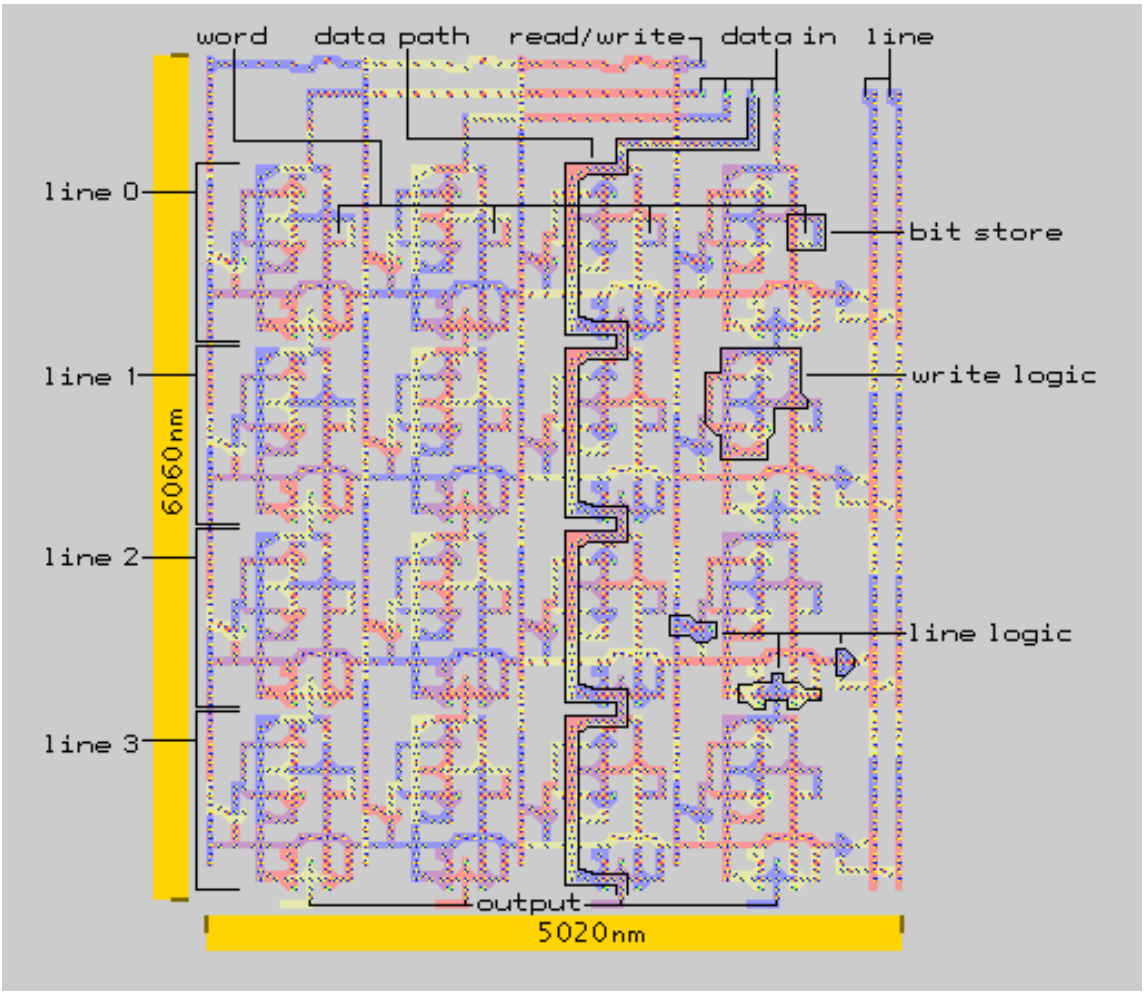

Fig. 8: The suggested design of a 4x4 QCA memory array

Each bit of data is stored in a small loop. Most of the circuit area is used by line selection and read/write capabilities. Throughout the circuit single plane signal crossing is achieved using rotated cells. AND, OR, and NOT gates are also found in the circuit's combinatorial logic. The input signals move from the top right to the remainder of the circuit. The output is at the bottom of the circuit.

The memory was tested with read and write operations. For example, in clock periods one through four, the numbers 0, 15, 5, and 6 were written to lines 0, 1, 2, and 3, respectively. In the fifth clock period, the circuit was sent a read from the last line, which

serves as a delay to give the circuit enough time to write. Then in periods 6-9 the circuit is told to read from lines 0-3. All of this information is shown in binary form in Table 1 including the simulation output. QCAS records dashes in the output when a cell is in either the release or relax clock phase.

Table 1
Simulation Results for the 4x4 Memory Array

Period	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Phase	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY	BPRY
line1	0000	0000	1111	1111	1111	0000	0000	1111	1111	0000	0000	0000	0000	0000
line0	0000	1111	0000	1111	1111	0000	1111	0000	1111	0000	0000	0000	0000	0000
in0	0000	1111	1111	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
in1	0000	1111	0000	1111	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
in2	0000	1111	1111	1111	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
in3	0000	1111	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
write	1111	1111	1111	1111	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
out0	11--	11--	11--	11--	11--	11--	11--	11--	11--	11--	00--	11--	11--	00--
out1	-11-	-11-	-11-	-11-	-11-	-11-	-11-	-11-	-11-	-11-	-00-	-11-	-00-	-11-
out2	--11	--11	--11	--11	--11	--11	--11	--11	--11	--11	--00	--11	--11	--11
out3	1--1	1--1	1--1	1--1	1--1	1--1	1--1	1--1	1--1	1--1	1--0	0--1	1--0	0--0

Because of the circuit design, there is a one period delay before newly written data becomes available for a reading operation. There is a 5 period delay after a read or write operation before the stored data reaches the output. In clock periods 11-14 the new data (0, 15, 5, 6) for lines 0-3 is displayed at the output. Because of the circuit design, the write operation also acts as a read operation, sending a line's old data to the output. In the clock periods 6-9, the old data from lines 0-3 show up at the output (15, 15, 15, 15) because of write operations. There is one situation where the circuit may write incorrect data. If a read command is sent one period after a write and the write is to a line below the read command line, the write will write data retrieved from the read instead of from the input. This error could be considered a feature; it is essentially a copy line command. To avoid this error, a command to read line 3 could follow the write command.

The QCA memory circuit may prove useful in future circuit designs. It can be scaled to store longer words and more lines without increasing the complexity of the design. It might be possible to increase the density of the circuit by rearranging the cells.

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