

## **Undergraduate Research in the Modeling and Simulation of GaAs-Based High-Speed Circuits**

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### **Abstract**

An undergraduate research site in the area of modeling and simulation of GaAs-based high-speed circuits is described. Undergraduate students worked with electrical engineering graduate students and faculty members for ten weeks on projects ranging from designing & study of GaAs-based circuits using MAGIC and L-Edit to modeling the very high-frequency effects and parasitic capacitances in the GaAs-based VLSI interconnections to computer simulations of GaAs-and SOI-based devices and circuits using the semiconductor TCAD tools. In this paper, the undergraduate research projects carried out by the REU students are summarized

### **1. Introduction**

It is widely recognized that active research experience is one of the most effective techniques for training and motivating undergraduate students for careers in science and engineering. In the USA, National Science Foundation (NSF) recognizes this and supports undergraduate research under two programs: a) Under their "Research Experiences for Undergraduates (REU) Supplements" program, NSF encourages principal investigators of NSF-funded research grants to include one or two undergraduate students in their existing projects; and b) Under their "REU Site" program, NSF provides funds to set up undergraduate research sites consisting of nearly ten students to work on state-of-the-art research projects under the supervision of a faculty member.

Continuous advances in integrated circuit technology have resulted in smaller transistor dimensions, larger chip sizes and increased complexity. There is an increasing demand for circuits with higher speeds and higher component densities. Because of its semi-insulating property and the fact that the mobility of electrons is an order of magnitude higher in Gallium Arsenide (GaAs) substrate than in the widely used Silicon substrate, GaAs has emerged as a preferred substrate for the development of very high-speed integrated circuits [1, 2]. In fact, during the last few years, GaAs technology has emerged

rapidly from basic research to device and circuit development. In addition, growth of GaAs on silicon (Si) substrate has met with a great deal of interest because of its potential applications in the new hybrid technologies. GaAs-on-Si unites the high speed and optoelectronic capability of GaAs circuits with the low material cost and superior mechanical properties of the Si substrate. The heat sinking of such devices is better since the thermal conductivity of Si is three times more than that of GaAs. This technology has expanded rapidly from material research to device and circuit development. In this paper, research projects carried out by the undergraduate student at the undergraduate research site on GaAs-based high-speed circuits set up at the Michigan Technological University are summarized.

## 2. Undergraduate Research Site

Funded by a three-year grant from the National Science Foundation, an undergraduate research site was established at the department of Electrical Engineering at Michigan Technological University in the area of GaAs based very high-speed integrated circuits. This site consisted of ten undergraduate students selected on a competitive basis from institutions all over the USA. Eligibility criteria for participation were citizenship or permanent residence of the United States and completion of at least two years in electrical engineering, physics, computer science, computer engineering or a related field with a grade point average of 3.0 or over. Major objectives of this REU site were:

- a) Enhancement of student experience, competence, confidence and self esteem by working on a state-of-the-art electrical engineering research project;
- b) Encouragement of students to pursue graduate studies in electrical engineering and to choose a career in microelectronics/VLSI research; and
- c) Improvement of student oral and written skills through written reports and formal seminar presentations.

In addition to the host institution, students were selected from Rutgers University, Binghamton University, Calvin College, University of Rochester, Michigan State University and University of Ohio. Undergraduate students worked with electrical engineering graduate students and faculty members for ten weeks on projects ranging from designing a GaAs-based floating point multiplier to designing GaAs-based circuits using L-Edit to modeling the very high-frequency effects in the high-speed VLSI interconnections to modeling of parasitic capacitances for complex interconnection structures to computer simulations of GaAs- and SOI-based devices and circuits using the various technological computer-aided design (TCAD) tools. Faculty interaction was maximum during the first few weeks and decreased as students became more and more independent in carrying out their projects. During the last week of the REU site, students submitted formal written reports and presented formal seminars on their projects.

### 3. Undergraduate Research Projects

#### 3.1 Modeling of Very High-Frequency Effects in the VLSI Interconnects

An REU student (SW) worked on a project whose goal was to study the effects of very high-frequency phenomena on the propagation delays in the metallic interconnection lines on the rapidly emerging GaAs-based high-speed VLSI circuits. A numerical model and the related software were developed that include the high-frequency effects such as the skin effect, conductor loss, dielectric loss and the parasitic capacitances for a system of parallel interconnections printed on the GaAs substrate shown in Fig. 1. The parasitic capacitances were determined by using the method of moments in conjunction with a Green's function appropriate for the geometry of the interconnections. The Green's function was calculated by using the method of multiple images.

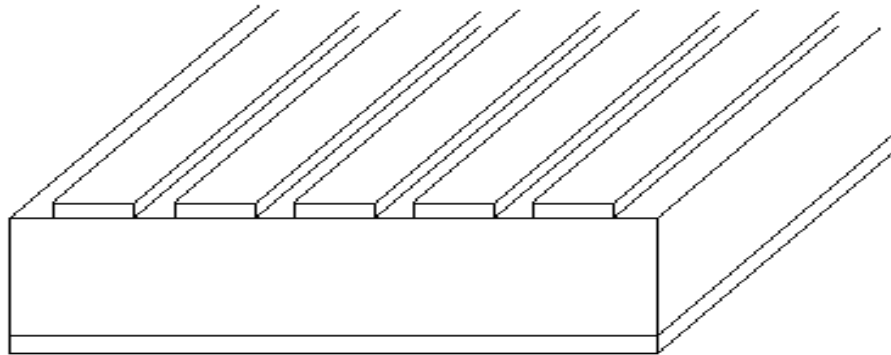


Fig. 1: Schematic diagram of the interconnection lines

The program was used to study the dependences of the propagation delays in the interconnections on their various design parameters such as their length, width and the material resistivity as well as on other factors such as the driving transistor's output resistance, loading transistor's input capacitance and the frequency of operation. For example, the dependence of rise time on the frequency showed that the frequency has a significant effect on the interconnection delay particularly at higher frequencies.

#### 3.2 Modeling of Parasitic Capacitances in the VLSI Interconnections

An REU student (NE) extended the Green's function method developed earlier to determine the ground and coupling capacitances for various systems of multiconductor and multilevel interconnections on a GaAs-based VLSI circuit shown in Fig. 3 below. He used this technique to study the dependences of these capacitances on the various system dimensions and other interconnection parameters.

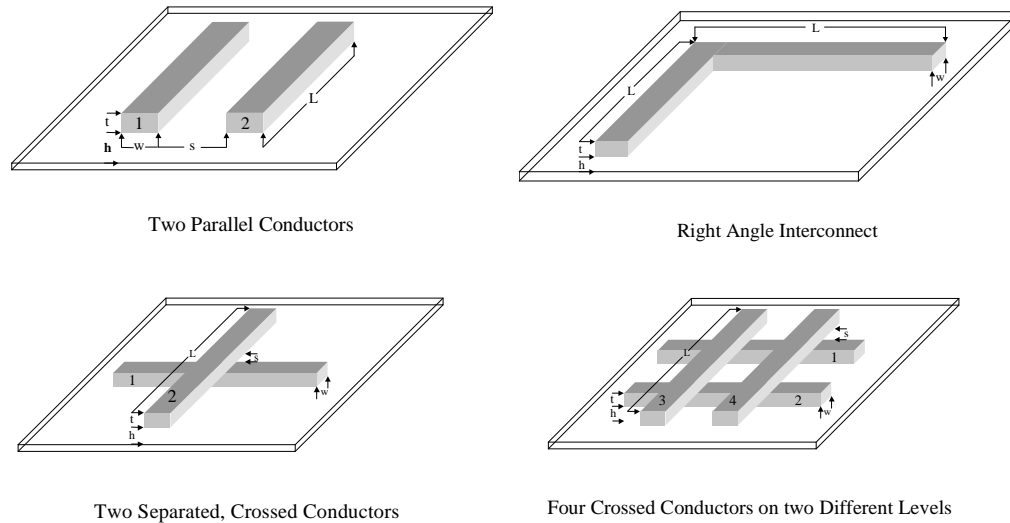


Fig. 3: Schematic diagrams of the four simulated conductor configurations.

### 3.3 Computer Simulation of GaAs and SOI Devices Using TCAD Tools

As device sizes shrink and new materials are added, it becomes more expensive, time-consuming and physically difficult to test each component and that device simulations using the semiconductor technological computer aided design (TCAD) tools is an economical alternative to experimental testing. They found out that the Silvaco Corporation's "Virtual Wafer Fab" (VWF) package consisting of process simulation software called ATHENA, device layout software called DevEdit, device simulation software called ATLAS and Tonyplot for displaying results could be used to simulate GaAs, SOI as well as conventional silicon devices.

Four REU students (JD, NS, PT, TD) used the TCAD tools to simulate the performances of several GaAs- and SOI-based devices as functions of device dimensions and other fabrication parameters such as impurity concentrations and annealing temperatures. First, they fabricated these devices in the virtual environment using ATHENA and then studied their operational characteristics using ATLAS. For example, for an SOI MOSFET, the dependence of the turn-on voltage on the annealing time is shown in Fig. 4.

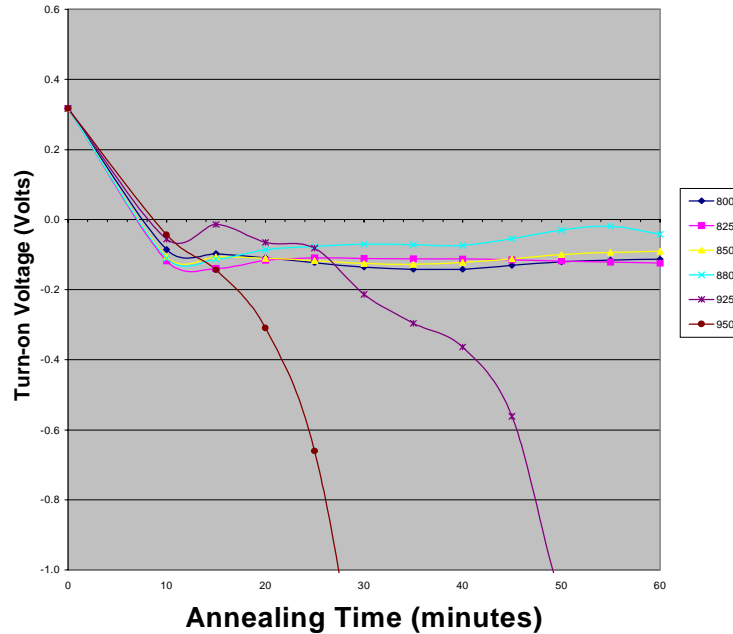


Fig. 4: Turn-on Voltage ( $V_t$ ) decreased with various annealing sequences for an SOI MOSFET.

### 3.4 GaAs-Based Floating Point Multiplier

Floating point calculations are critical to modern computer systems for applications ranging from graphic intensive games to neural networks. Two REU students (EL JE) recognized the superior characteristics of GaAs over silicon and designed a 32-bit GaAs-based floating point multiplier. As shown in Fig. 5, the design of the multiplier has three specific parts: the exclusive-or gate for the sign bit, the carry-lookahead adder for the determination of the exponent, and the multiplier for the mantissa.

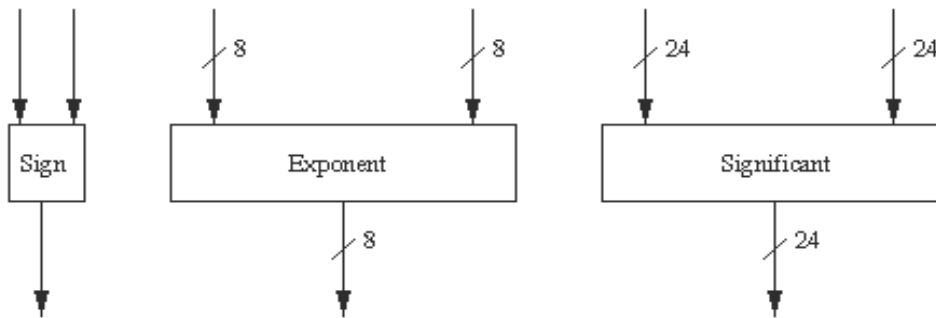


Fig. 5: Block diagram of the multiplier design.

Performance of each component of the design was simulated using SPICE and the performance indicators for the entire circuit were predicted. The performance of this multiplier shows that GaAs is a viable and realizable technology for VLSI design. By extracting components of the design layout they estimated a total of 12.5 ns delay time for the entire circuit using SPICE.

### 3.5 Designing GaAs-Based Integrated Circuits Using L-Edit

IC design tool called L-Edit developed by Tanner Research is used primarily for designing Si CMOS circuits. In this project, two REU students (SD, RM) extended its ability to designing GaAs-based ICs. This was done by developing a GaAs technology file. The GaAs circuits designed were simulated by using S-Edit and the waveform generator. The picture below shows these two REU students presenting their seminar.



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### **ASHOK GOEL**

Ashok Goel received his Ph.D. degree from The Johns Hopkins University in 1987. Currently, he is an Associate Professor of Electrical Engineering at Michigan Technological University. He is the author of a book "High-Speed VLSI Interconnections" published by Wiley Interscience in 1994. His research interests include nanotechnology circuit design and GaAs-based integrated circuits. He is a senior member of the IEEE.

MARTHA SLOAN

Martha Sloan received her Ph.D. degree from the Stanford University. Currently, she is a Professor of Electrical Engineering at the Michigan Technological University. She is the author of several books. She has served as President of the IEEE.

JASON DECKER

Jason Decker was a visiting undergraduate student from the Binghamton University.

STEPHANIE DRAGER

Stephanie Draeger was a visiting undergraduate student from the Michigan State University.

TREVOR DUPRAS

Trevor Dupras was an undergraduate student at Michigan Technological University.

NURI EADY

Nuri Eady was an undergraduate student at Michigan Technological University.

JEFF ESPENSCHIED

Jeff Espenschied was a visiting undergraduate student from the University of Ohio.

EUGENE LEE

Eugene Lee was a visiting undergraduate student from the University of Rochester.

REBECCA MORRISON

Rebecca Morrison was a visiting undergraduate student from the Rutgers University.

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Nicholas Sze was a visiting undergraduate student from the University of Rochester.

PAUL TOTH

Paul Toth was an undergraduate student at Michigan Technological University.

STEPHANIE WEITMEYER

Stephanie Weitmeyer was a visiting undergraduate student from the Calvin College, Grand Rapids, Michigan.