AC 2009-1891: USE OF A SIMULATION SWITCH MATRIX FOR EFFICIENT DESIGN OF CMOS ANALOG INTEGRATED CIRCUITS

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Use of a Simulation Switch Matrix for Efficient design of CMOS Analog Integrated Circuits

Abstract

CMOS analog integrated circuit (IC) design is a technology-dependent process. Analog design follows a process for which transistor sizing is necessary to achieve performance goals that are defined by a series of simulation tests. Both the design and the pedagogical processes make use of one or more algorithms in which a set of subcircuits are separately tested and then linked together into an integrated cell design, usually that of the 8-transistor operational transconductance amplifier (OTA).

This paper identifies a technique that reduces much of the extra design overhead by framing the OTA as a single schematic who test configurations are controlled by a simulation version of a switch matrix. The switch matrix (1) links a set of independent sources and loads to the circuit under test and (2) reconfigures the test topology of the circuit.   The new technique is of value to both the instruction process and the circuit designer since it is simple and direct.   Given the simplicity it is also possible to compare effects of different technologies, usually by a collateral use of a spreadsheet utility and its graph capabilities.   The student version of Cadence/ORCAD/pSPICE is the principal simulation design utility, with the Excel platform as a complementary utility.

I. Introduction

In the integrated circuit world, the circuit designer cannot limit his/her skills to logic circuit applications alone. Much of the custom and semi-custom nature of logic circuit is, in fact, resolved more directly by gate arrays and standard cells. And at higher levels logic circuit design is more likely to be dominated by embedded systems and DSP (digital-signal processing).

On the other hand the analog design environment is strongly contingent on the specific application, most of which relate to frequency and feedback requirements. The increased market emphasis on RF (radio-frequency)-linked systems that relate to such environments as Bluetooth and ZigBee has demanded more and more analog skills to successfully negotiate the evolution in MOS and MOS-related technologies.

Analog design is a science that relates most strongly to differential equations since it is defined primarily in terms of an interaction between slopes and loads. The transfer functions are slopes in the voltage domain; the frequency functions are slopes in the time and phase domains.

Passive analog systems give transfer ratios (slopes) that are less than unity and frequency responses that are defined by damping factors. Active systems, for which power is incident either as RF (radio-frequency) energy or available as steady-state energy (usually disguised as power rails) will have transfer slopes greater than unity and frequency responses for which stability and resonances are of concern.

The circuit designer usually operates in a design environment for which the device technology is pre-defined and therefore it determines the basic deign constraints such as voltage threshold and recombination effects. In a more mature setting the circuit designer may be able to influence the fabrication process but usually only in the sense of choice between one technology process and another. The principal design parameter is therefore device size, and is used to accommodate many of the device constraints, as well as adjust offsets and operational current levels.

The decision process relates primarily to basic physical models of the MOS transistor, which are based on devices of much larger dimensions and much lower fields. In order to make any kind of predictive analysis, these basic models benchmark the process and therefore some predictive simulations are necessary. These are best manifested in such constructs [1] as a CMOS pair for evaluation of the transconductance, g_m and of the drain conductance g_{DS} slopes. The device test topology is represented by figure 1-1(a). The simulation results are as shown by figure 1-1(b).
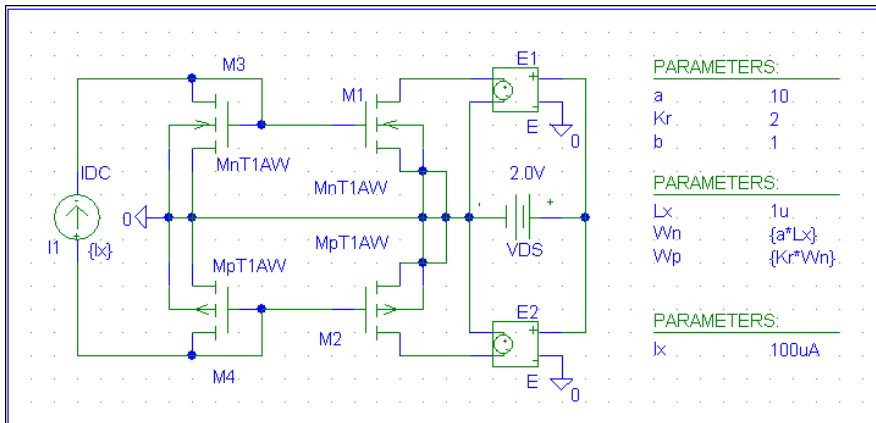
Figure 1.1(a) Schematic of a CMOS pair (nMOS and pMOS transistors) as needed for physical assessment of operating characteristics. In this case the transistors are configured for assessment of the <u>drain conductance</u> ($g_{DS} = dI_D/dV_{DS}$). The PARAMETER statements to the right are used primarily to define transistor sizing $Lx =$ channel length, $Wn =$ width of nMOS transistor, and $Wp =$ width of nMOS transistor. Transistors M1 and M2 are the devices being examined and are biased by transistors M3 and M4, respectively.
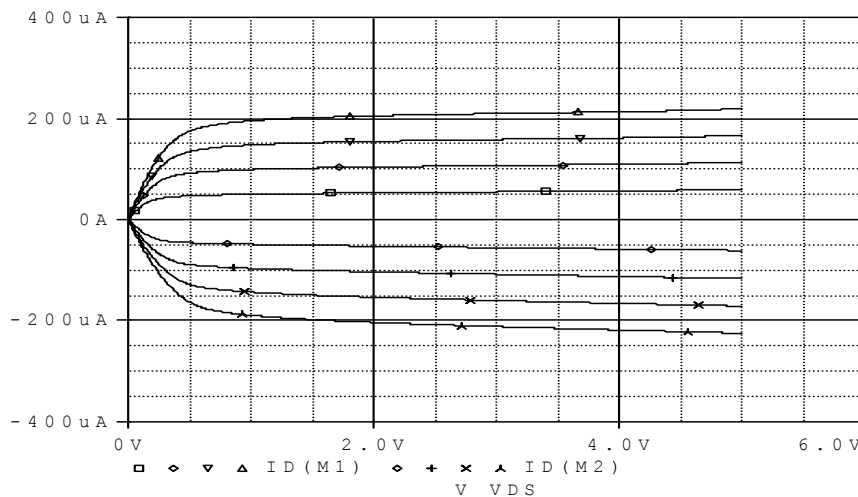

Figure 1.1(b) Simulated I_D-V_{DS} (current-voltage) characteristics of CMOS-pair of transistors. The positive values of current are those for the nMOS transistor (M1 in figure 1.1(a)) and the negative values of current are for the pMOS transistor (M2 in figure 1.1(a)).

Figure 1.1(b) is the result of simulation of a device defined for a 0.5 micron technology, in this case the technology defined by a particular MOSIS [2] run. The simulation model used for this technology, known as the BSIM3V4 [3,4] model is one which accommodates high-field effects but is otherwise fairly impenetrable to analytical definition, other than a few first-order parameters such as VTO (threshold voltage) and low-field mobility (U0) that appear in its parameter file. The BSIM-4 model addresses the process and second-order field effects. Most of these effects are negligible at the lower-field (large device dimension) level but are essential at the sub-micron technology level.

The predictive analysis requires extraction of the slope $g_{DS} = dI_D/dV_{DS}$ for an expected and elected operational level such as $V_{DS} = 2.0$V, as is represented by figure 1.2.
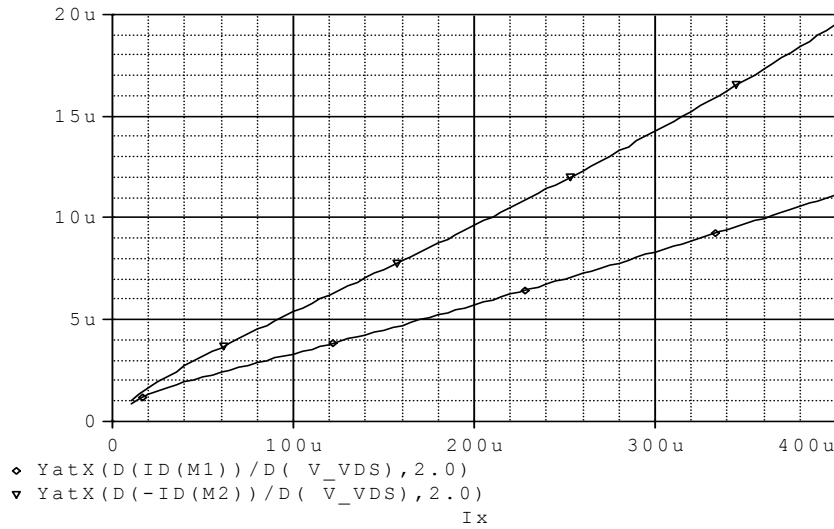

◇ YatX(D(ID(M1))/D(V_VDS),2.0)
▽ YatX(D(-ID(M2))/D(V_VDS),2.0)
                        Ix

Figure 1.2: Semi-empirical behavior of drain-conductance g_{DS} at $V_{DS} = 2.0$V as a function of drain current I_D for both nMOS and pMOS devices and *W/L* (size) ratios defined by the parameters tables of figure 1.1(a). To first order this behavior is linear, consistent with the physical model.

This figure is one for which goal function [1] features of the simulation postprocessor are applied, and may in turn be used to devise an empirical analytical model of g_{DS} as a function of I_D, which is usually one of the design parameters. An empirical model would most likely be defined by capture of the g_{DS} data of figure 1.2 into a spreadsheet, where empirical relationships can be assessed (and often are undertaken as a classroom exercise).

Figure 1.2 represents the reason why an extensive set of simulations are necessary. It represents the extraction of the basic behavior of the transistors and the linearity of a slope function that directly defines transfer characteristics for an analog circuit. It shows that g_{DS} is slightly non-linear, and will effect some distortion of the signal transferred by this circuit.

II. The 8-transistor OTA (operational transconductance amplifier)

The basic requirement of the operational amplifier (opamp) and its integrated circuit equivalent, the OTA is that it be a differential amplifier with large voltage gain. Values on the order of 2000V/V (66dB) or more are typical. Large gain is a necessary since the OTA is always used in a negative feedback mode. The output and input signals then are then defined entirely by the feedback network. Feedback networks are usually linear components, and thereby the feedback construct provides a linear transfer function. For reasons of distortion and problems with signal aliases, linearity is essential for RF and audio systems.

The OTA is the front end of an opamp and is expected to be an integrated circuit construct or 'cell' that will connect only to high-impedance internal loads. Therefore the output impedance of the OTA does not have to be low as does the opamp and so OTA relaxes many of the circuit requirements and simplifies its construct.

There is a selection of OTA constructs, with choice depending on the working environment. If voltage supplies are large, then more transistors may be stacked to take achieve the higher performance effects. Often a single high-gain differential stage of the form of a cascode OTA will suffice. If the power rails are low-impedance, then larger currents and higher speed topologies can be supported. And there are OTA topologies suited only to micropower operation.

But in all cases there are performance requirements and specifications that are used to define the construct. Some of these specifications relate to distortion; some relate to stability; some relate to overshoot. The process whereby these requirements are addressed is systematic, and form the essentials of the OTA design algorithm.

The simplest and most direct form of the OTA and the one most commonly applied in the integrated circuits environment is represented by figure 2-1. This OTA topology is usually defined as the '8-transistor OTA'. Its first stage is a source-coupled (differential) pair and its second stage is of the form of a common-source a CMOS amplifier. The overall gain of these two stages is on the order of 6500 V/V.
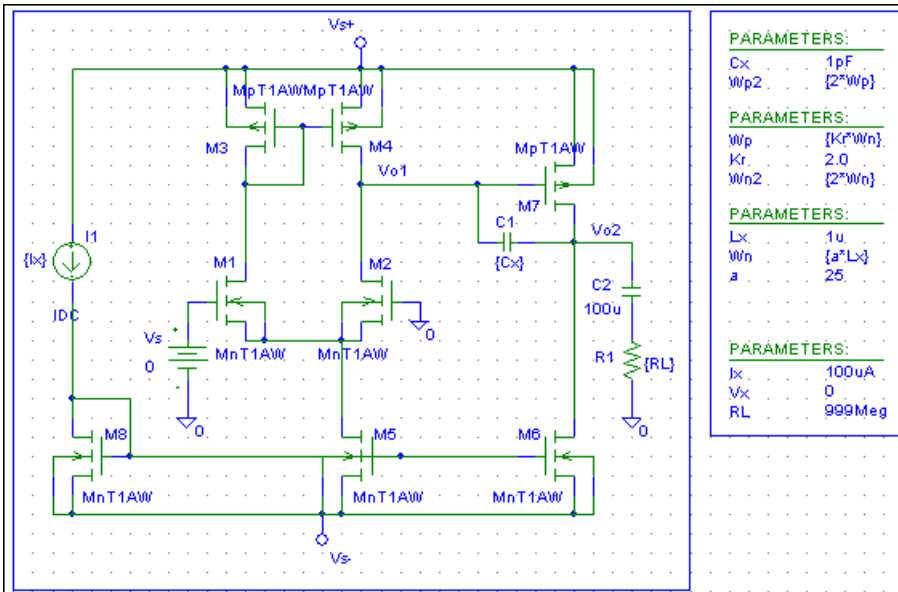
Figure 2-1. The 8-transistor OTA. Transistors M1, M2, M3, and M4 are the first-stage source-coupled pair, for which M5 and M8 form a current source, and transistors M6 and M7 form the second stage for which M8 and M6 provide an active load for transistor M7.

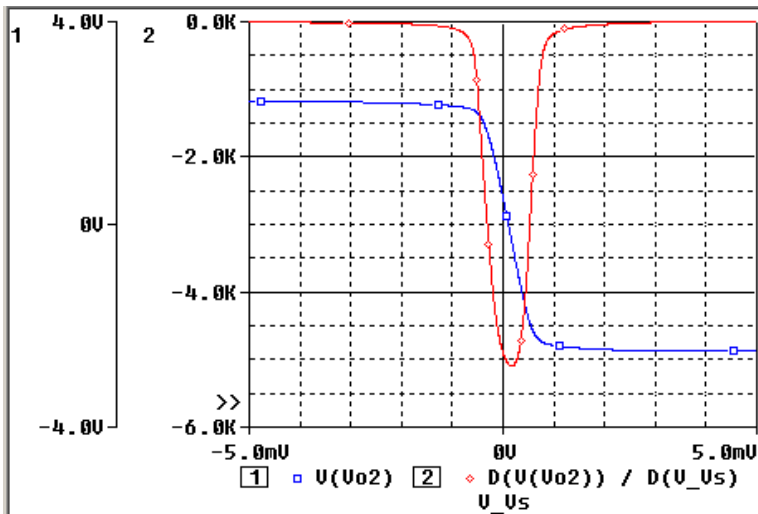Simulation results for voltage gain of this circuit are shown by figure 2-2.

Figure 2-2. Simulation of the transfer characteristics of figure 2-1. Note that the transfer gain (= slope) is approximately -5100 V/V. The sizes of M6 and M7 are preselected to minimize input offset problems, for which transfer gain is centered about $Vin = 0$.

Confirmation of high transfer gain is the initial condition for the OTA design. But the actual measure of transfer gain is not as critical as are others that relate to distortion, bandwidth, output swing and stability. It is only important that the transfer gain be large.

Otherwise, the performance specifications and terms that define OTA transistor and component sizes are summarized by table 2-1:

	Specification	Interpretation	Adjusted by	requirement	Defined by
1	Slew rate	$\dfrac{dV_{out}}{dt} \cong \dfrac{Ix}{C_x}$	Ix or Cx	maximize	application
2	Gain-bandwidth	Frequency at which gain = unity	Cx and M9	maximize	application
3	Phase margin	180° – phase shift at unity gain freq	Cx and M9	$\phi > 75^o$ for min. overshoot	stability requirement
4	Output floor	Lowest V(out) with no distortion	Ix and M6	minimize	application
5	Output ceiling	Highest V(out) with no distortion	Ix and M7	maximize	application
6	Input common-mode range	Upper and lower limit of V_{in}(DC level)			
7	Input offset voltage	Maximum gain offset due to mismatch	M7	minimize	operational
8	Power budget	$2*Ix*(Vs+ - Vs-)$	Ix and V(supply)	minimize	general, and application

Table 2-1: Performance criteria for the (8-transistor) OTA design.

These specifications are applied in the order of importance to the application. Some of the caveats, such as symmetry and size consistency are not listed. For example, it is essential that M1 and M2 be the same size and that M3 and M4 be the same size in order that the output of the first stage (the source-coupled pair) be balanced about the zero input level. Circuits in which these components are not equalized have a hysteresis and have application as a comparator (compares two inputs) rather than as an OTA.

Device sizes (transistor and capacitance) must also be kept as small as possible in order to limit the silicon real estate required. An OTA with minimal performance specifications is expected to occupy a relatively small footprint and demand very little power budget. Higher-performance OTA constructs and discrete operational amplifiers may given considerably more silicon area and power levels.

Requirement (3) (= phase margin) is probably the most challenging design commitment, since it must not only accommodate the circuit but also the possibility of a large capacitance load. It is also the requirement for which overshoot must be minimized, should the OTA be used for digital applications. Overshoot will be eliminated if the phase margin is greater than 75° [5,7]. Phase margin is adjusted by means of capacitance Cx and by addition of an extra transistor (M9) as represented by figure 2-3.
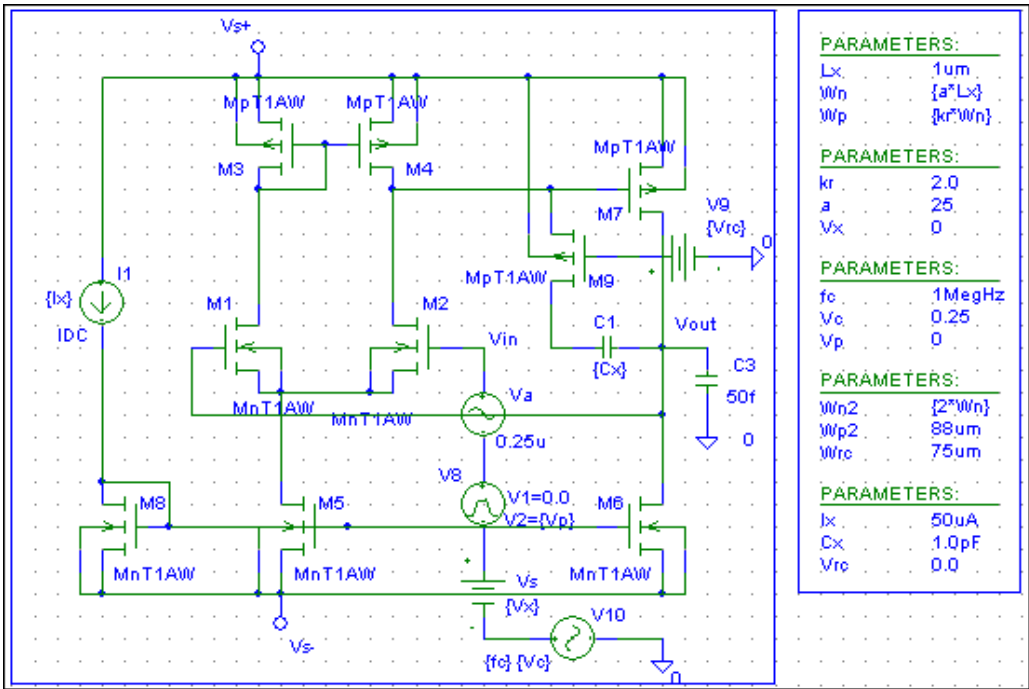
Figure 2-3. 8-transistor OTA with phase adjustment transistor M9. M9 must be externally biased into an operational mode consistent with transistor M7. The external biasing circuit (not shown), also called a constant-transconductance bias circuit, also defines current source (Ix) level. Its formulation is separate to the OTA design algorithm.

Background knowledge or classroom dialogue is assumed. Requirements (1) thru (8) are the basis for the design algorithm of this simple, functional and important circuit topology. From these requirements the design algorithm should not only identify the transistor(s) or component sizes necessary to meet or trade-off a given specification, it also should also identify the best order for which devices are sized and the iterative procedures thereto.

III. OTA test frame and algorithm using the 'software switch matrix'

The OTA test frame is shown by figure 3-1. The switch matrix is to the right. It consists of three single-pole double throw (SPDT) switches. Each SPDT switch two connection paths (1) a normally-closed resistance path and (2) a normally-open resistance path. These connection paths are represented by resistances *Rnc* and *Rno*, respectively. Two of the SPDT switches are linked together to form a bastardized version of a double-pole, double-throw (DPDT) switch.

Each switch has two paths. Path resistances are of the form:

$$Rnc = (1n + swn*1G) \qquad \text{and} \quad Rno = 1/(1n + swn*1G)$$

Rnc represents the 'normally closed' resistance. *Rno* represents the 'normally-open' resistance. If the 'switch toggle' *swn* = 0, (= normal), then *Rnc* = 1nΩ and *Rno* = 1GΩ, which are very reasonable approximations to those of a real switch. If *swn* = 1, then *Rnc* = 1GΩ, and *Rno* = 1nΩ and the connectivity of the paths are switched.

The switches are controlled by switch matrix 'toggles', *sw1* and *sw2*. Toggle *sw1* toggles two SPDT switches simultaneously as the attempt at forming a DPDT equivalent.
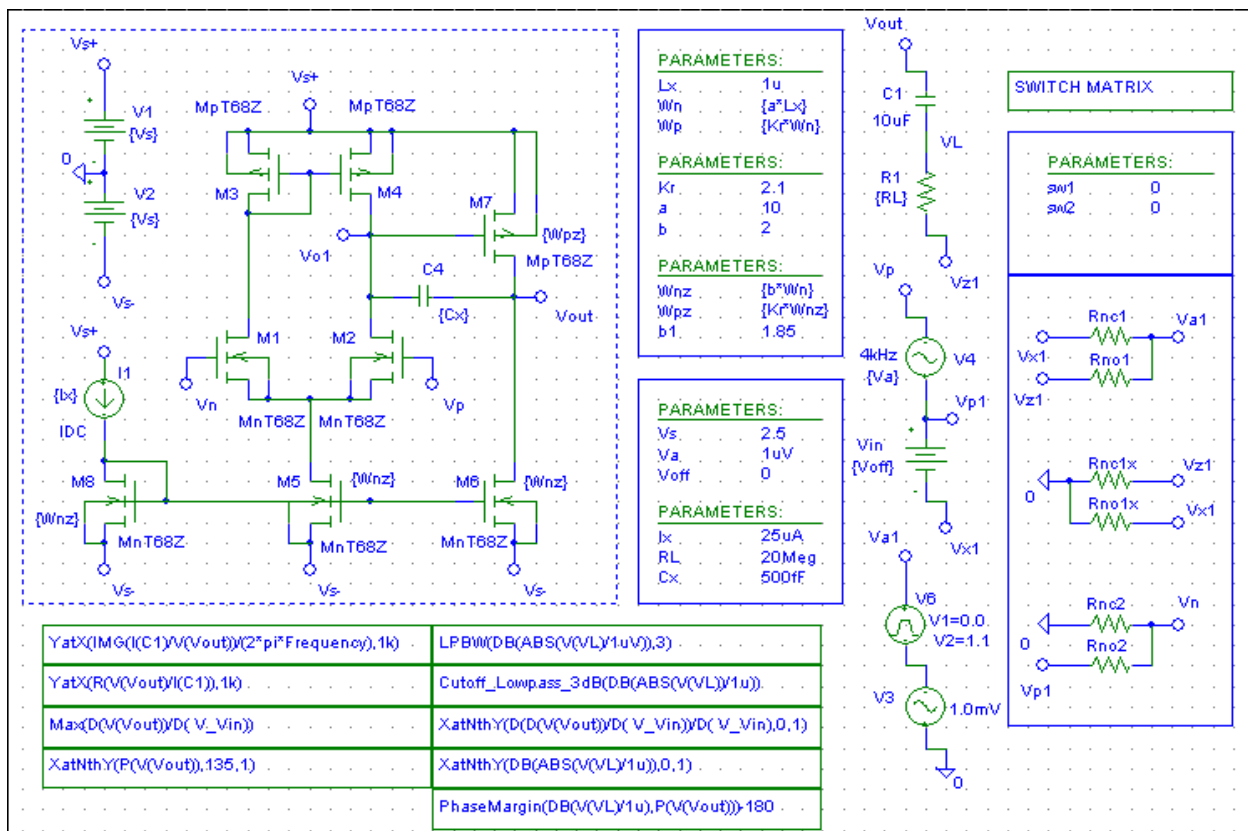

Figure 3-1: Source-loaded 8-transistor OTA test frame. The topology is a complete design and will be layout ready once the device and component sizes are defined.

With the switches *(sw1, sw2)* set as shown, source *Va1* is connected to node *Vx1*. This node is the portal for two test sources *Vin* and *V4* that connect to OTA input *Vp*. Node *Vn* of the OTA is connected to ground. Output node *Vout* is connected through load R_L and C_L to ground since *Vz1* is connected to ground.

Initial assumptions are:

(1) Transistors M1 = M2 = M3 = M4. All have a common length, *Lx*, (in this case = 1.0um). Transistors M1 and M2 are sized by (parametric) width *Wn*. Transistors M3 and M3 are sized by width *Wp*. Values are specified by the first and second parameter lists of figure 4-1. The second parameter table chooses aspect ratio *kr* = 2, specific to the elected technology, for which the nMOS transistors are intrinsically 2.0 more conductive than the pMOS transistors.

(2) Transistors M5 = M6 = M8 are sized by (parametric) width *Wn2*. The value of *Wn2* is expected to be approximately 2*Wn* since transistor M5 carries twice as much current as either M1 or M2. Transistor M7 is sized by width *Wp*. It is expected to be approximately of width = 2*Wp* for a balanced output, subject to adjustment to minimize input offset voltage.

The OTA Design Algorithm:

Step 1: The first step of the design algorithm usually relates to performance criterion #8 of table 2-1, the power budget. In this example voltage rails (not shown) are (+,-) 2.5V and the choice of *Ix* = 50uA represents approximate level of power consumption of 2 x 50uA x [-2.5-(-2.5)] = 500uW. In the assessment the current path associated with current source I1 and transistor M8 is omitted. It will be replaced by a constant transconductance bias circuit, which has a separate power budget and is shared by more than one OTA. The witch matrix is set with *(sw1, sw2)* = (0,0) and will remain at this setting for the first 5 steps.

Step 2: Once *Ix* is defined, sizes of the transistors M1 – M6 may be identified by equation (2-5). For *Wn* = 25um the limiting factor *ΔV* is expected to be less than 0.2V for transistors M5 and M6, which are the critical devices in defining output floor (criterion 4) and the common-mode input range (criterion 6). Since size relates to *W/L* (equation 2-3) a ratio parameter *a* is used instead of size in um.

Step 3: The first simulation sweeps DC source *Vs* (see figure 4-1) from –5mV to +5mV. All other input sources are inactivated. This sweep evaluates the transfer gain, and the sweep response would be similar to figure 3.2. Concurrently the value of *Wp2* is stepped over a small range centered at approx. *2Wp* (for this example would be = 100um). The value of *Wp2* for which the peak falls at Vs = 0 will minimize the input offset (criterion 7). Figure 4-2 shows the test with *Wp2* stepped over three values. Once this value is determined it is inserted as a fixed value in the parameter listings, which, as represented by figure 4-1, becomes *Wp2* = 88um.
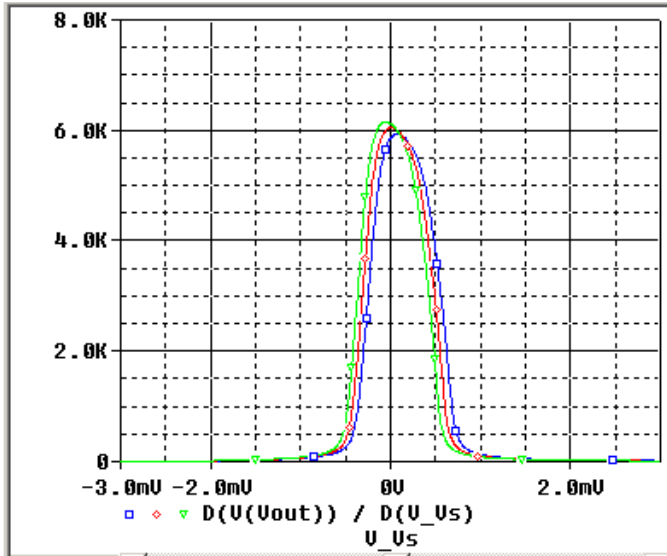
Figure 3-2: Step 3 = simulation to minimize input offset voltage by adjustment of the size of transistor M7. In this illustration *Wp2* is stepped by 5um from 80um to 90um.

Step 4a: Capacitance *Cx* is used to compensate the OTA for stability. It accomplishes this task by shifting the circuit frequency response to a form called a "single-pole" response for transfer gain magnitudes greater than unity. The level of gain = 1.0 (also called the '0-dB' gain level') is the highest useable gain level of the OTA.   The frequency at which this occurs is called the 'unity-gain frequency' = f_T.

Other than stability, the single pole response rolls off with slope –1.0V/V (also called a –20dB per decade slope). So anywhere along this slope the product of gain and bandwidth is a constant, which = f_T since unity gain is also along this slope. So f_T is therefore also called the gain-bandwidth product (GB). It is desirable that f_T be reasonably large.

The simulation test is accomplished by activating the AC voltage source *Va*. This source must be given a relatively small amplitude since the voltage gain indicated by figure 3-2 is large. In this case the amplitude is chosen to be 0.25uV. The AC source is then swept over a large range, in this case from 1kHz to 1000MegHz, which is a typical frequency sweep for an unknown behavioral response. Capacitance *Cx* is usually stepped through several values until the slope -20dB/decade is accomplished for all vales of gain > 1.0, as represented by figure 3-3(a).
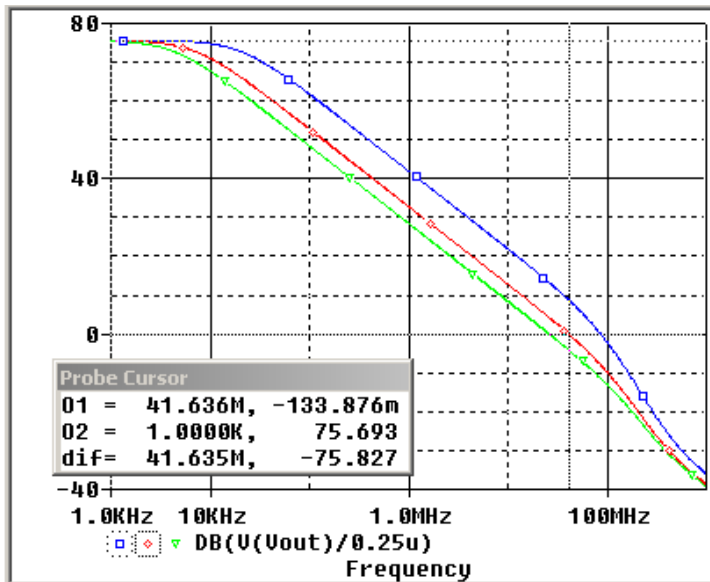
Figure 3-3(a): Frequency sweep of the OTA construct, with *Cx* stepped from 0.5pF to 2.5pF. The lowermost (green) trace corresponds to *Cx* = 2.5pF and is linear for all gain values > 0 dB (same as unity gain) but at the expense of a larger capacitance. The cursor is set to the 0dB level for the *Cx* = 1.5pF trace and shows a gain-bandwidth f_T = 41.6MHz. This simulation is sensitive to the size and bias of compensation transistor M9 so this step may be subject to iteration after transistor M9 is adjusted in a later step.

In this case a value of *Cx* = 1.0pF is the minimum capacitance needed. It happens to be the same as the initial guess, but if not, the new value should then replace the *Cx* (initial) = 1.0pF value in the parameter listings. Capacitances typically occupy a significant amount of silicon real estate and so it is desirable that they be kept as small as possible.

Step 4b: (Initial assessment of the phase margin). This step can be accomplished concurrently with step 4a since it is associated with the same simulation. All that is necessary is that the phase shift plot for *Vout* be called up and overlaid on the magnitude plot. At the frequency for which the gain is unity, which in this case is f_T = 57.8MHz (for the trace corresponding to *Cx* = 1.0pF), the value of phase margin PM = 180° − ϕ, which in this case = 39° since ϕ = 141.02°.

PM = 39° is an insufficient phase margin for stability for most feedback topologies. The size of Cx is critical in defining the phase margin. If *Cx* = 2.0pF been chosen the PM would have been approximately 60° but would require twice as much real estate.
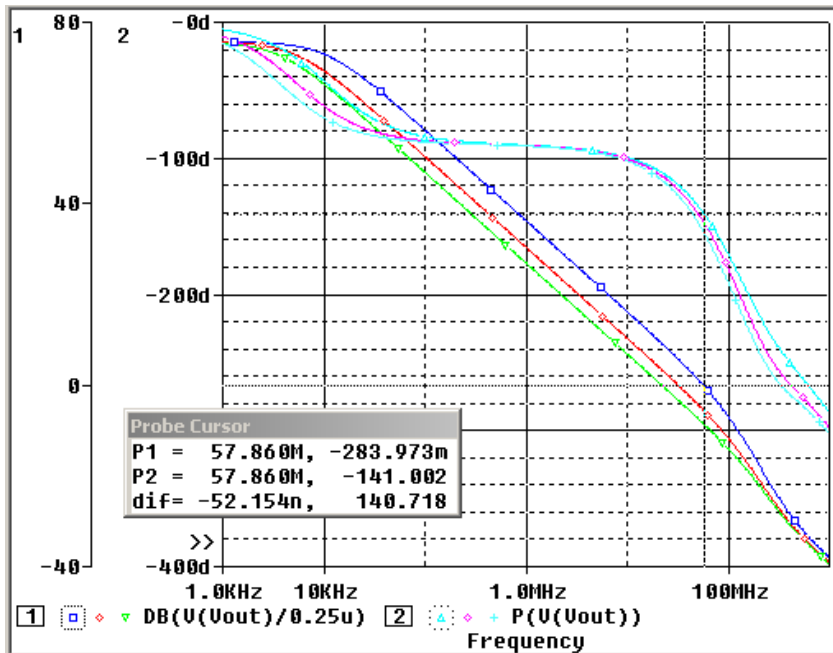
Figure 3-3(b): Measurement of phase margin (PM) with *Cx* stepped. Cursor #1 is aligned to frequency f_T, (unity gain frequency). Cursor #2 is linked to the corresponding trace for phase shift *P(Vout)* and aligned to this frequency. The phase shift at f_T is the y-axis value for cursor #2. For this example *Cx* was stepped from 1.0pF to3.0pF in step of 1.0pF. The two cursors are linked to the traces for magnitude and phase corresponding to *Cx* = 1.0pF.

The assessment and adjustment of phase margin is the major challenge in OTA design and often requires iteration. As identified in step 4, frequency response and its corresponding phase shift is dependent on both *Cx* and on transistor M9. If we desire both high f_T and small *Cx*, the next step requires adjustment of transistor M9.

Step 5a. Transistor M9 has the effect of shifting phase without appreciably shifting f_T. It is assessed by frequency sweep, using source *Va*, with the same settings as in step 4. The size of M9, defined parametrically by *Wrc*, is stepped through several values. The nominal size of M9 is expected to be about the same as M7.

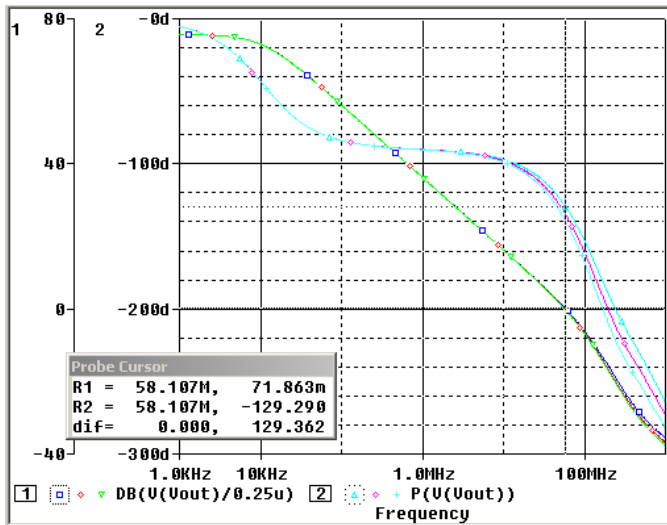The results of a simulation for which *Wrc* is stepped are shown by figure 3-4.

Figure 3-4. Adjustment of phase margin (PM) with size of M9 stepped.   In this simulation, *Cx* was chosen by step 4 to be = 1.0pF. The size parameter for M9, *Wrc*, was stepped from 75um to 95um. At *Wrc* = 75um, phase margin PM = $180^o – 129.2^o = 50^o$, an improvement over figure 3-3(b) of about 10°.

Step 5b: The conductance of transistor M9 defines its ability to shift phase, with lower conductance corresponding to lower phase shift and higher PM. This phase shift is also sensitive to the gate bias *Vrc* applied to M9 as illustrated by figure 3-5.
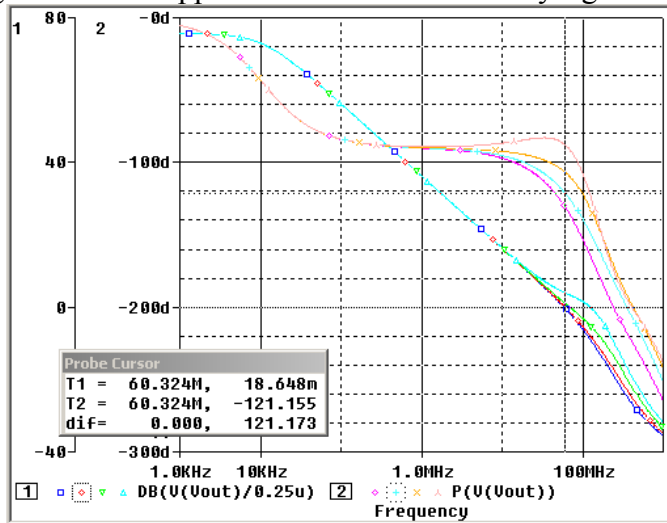

Figure 3-5. Adjustment of phase margin (PM) with bias of M9. Capacitance *Cx* = 1.0pF and *Wrc* = 75um. Gate bias *Vrc* is stepped from 0 to 0.15V and at *Vrc* = 0.05V, PM is approximately 59°.

Take note that adjustment of *Vrc* will produce a strong change in PM, but it also tends to distort the magnitude response. In the interests of a reasonably linear roll-off, *Vrc* must be kept fairly low. The *Vrc* bias is provided by the external bias network, which will be able to track phase behavior with respect to variations in the power rails.

Step 6: The next test is one for which the overshoot at maximum feedback is evaluated. This assessment is accomplished by activation of the pulse source V8. If the overshoot is within acceptable margins then this test is also used to assess slew rate *dVout/dt*.

This test calls for a complete reconfiguration of the test topology of the OTA schematic (figure 3-1). This is now accomplished by changing switch setting to (*sw1, sw2*) = (1,1). The effective alteration is shown by figure 3-6a. It also defends the odd topology of figure 3-1 for which this option was mildly emphasized. The simulation of the pulse output is shown by figure 3-6b
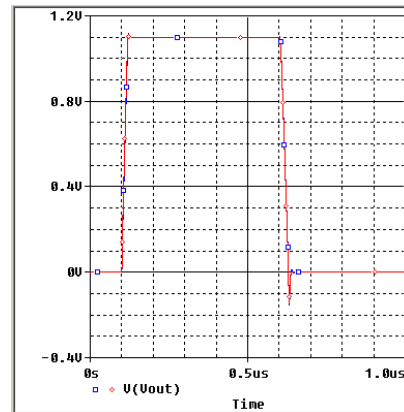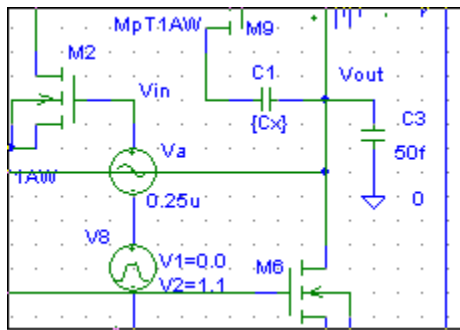

Figure 3-6a: Modification of figure 3-1 for 100% feedback (*Vout* connected to –*Vin*).

Figure 3-6b: Time sweep of (pulse). The input pulse, provided by source V6, is nearly ideal pulse width 0.5us and rise time1.0ns.

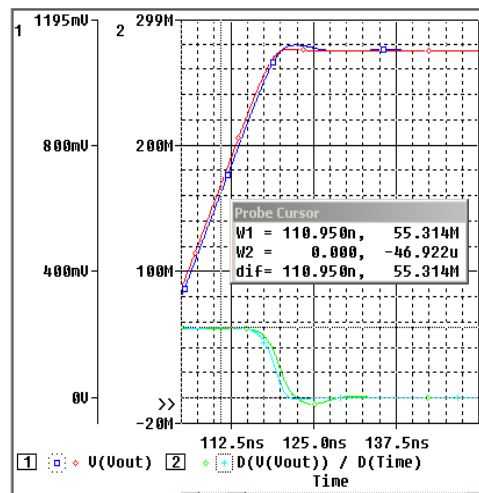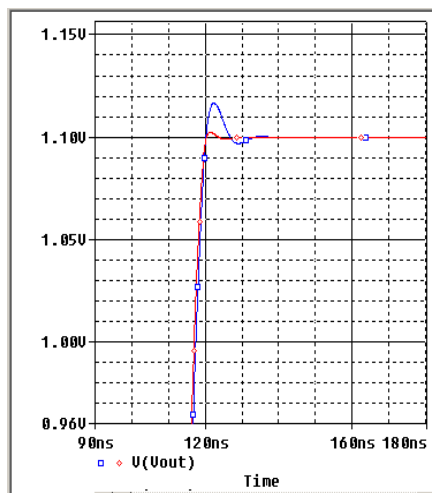**Figure 3-6c:** Zoom to leading edge of pulse, showing overshoot. The trace with the larger overshoot corresponds to *Vrc* = 0.0V.

Figure 3-6d: Derivative trace *dVout/dt* included and shows a slew rate (*dVout/dt*) = 55.3V/us.

The good slew rate is a consequence of having chosen *Cx* as small as possible within the limits imposed by the frequency domain analysis and stability requirements.

Step 7: The final performance assessment of the OTA is identification of its output range (Criteria 4 and 5) and its common-mode input range (criterion 6). Both of these are accomplished by source V4, which is activated by setting *Vc* non-zero. Since this is a time-dependent source, as is source V6, then V6 must be turned off by making *Vp* = 0.

Step 7a: Assessment of the output floor and ceiling, also called the 'swing' is not adjustable, but an assessment is a part of the test procedure. If *Vc* is equal or greater than the power rails, then the output will be amplitude limited. The onset of distortion is when the output swing *Vout(t)* begins to show distortion. This effect is illustrated by figure 4-7.
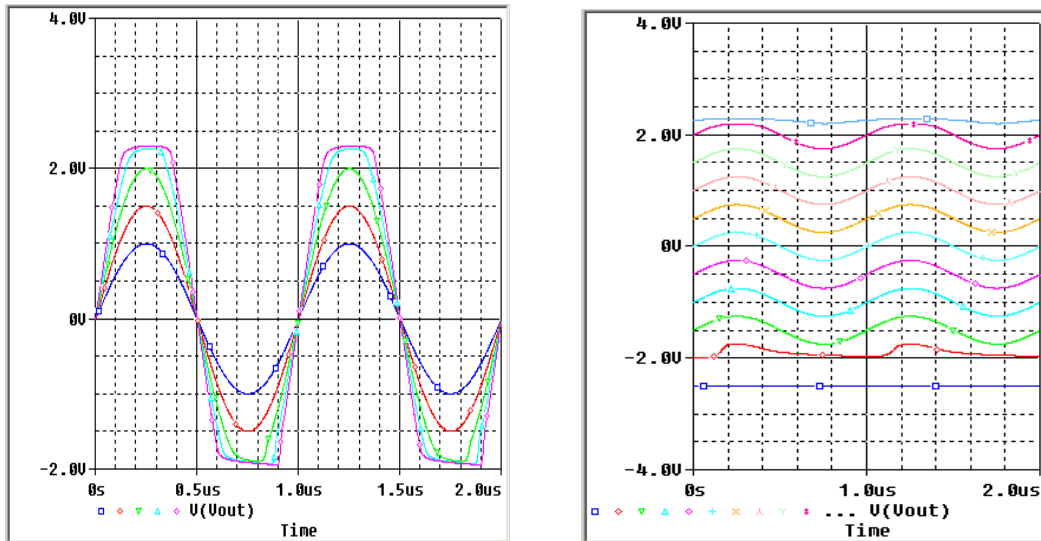

Figure 3-7: Limiting effects of output transistors. The *Vout*(ceiling) is approximately 2.1V and the Vout(floor) is approximately –1.7V.

Figure 3-8: Assessment of the limit effect of the input stage (common-mode range). In this case it is completely masked by the output compliances.

Step 7b: The common-mode input range is assessed by a low-amplitude signal on source V3 with *Vs* (= DC source) stepped from limits defined by the power rails. It is similar in form to the test of Step 7a, and often is masked by the output compliances, as shown by figure 3-8.

Steps 1 through 7 register a complete design algorithm for the 8-transistor OTA. The topology is laid down without exposition so that it may cut to the chase of the design process. The referral to table 3-1 provide the benchmark criteria for tuning and adjusting specifications.

The resulting performance factors of the OTA example, as designed under the T1AW 0.5um MOSIS process are

    (1) gain-bandwidth product 50MHz
    (2) slew rate 50V/us, and
    (3) zero-frequency gain 6000 V/V (75 dB)

This design would be adequate for most RF (radio-frequency) transceiver applications.

IV. **Conclusions and summary**.

Algorithms are a means to (1) reduce the length of the learning curve and (2) yield better efficiency in the design process. This algorithm includes a switch matrix that provides a very effective complement to the algorithm.

The instruction process for analog circuit design tends to be oriented toward subcircuits. Consequently the example of an inclusive circuit topology such as the OTA makes a good vehicle for the realization of integrated perspective. And the more mature circuit designer can focus on the parts rather than on the goal, provided that the process is efficient. The extra efficiency is afforded by the switch matrix.

Analog integrated circuits, as a classroom subject, is as much a software workbench as a pedagogical one. The impact of this new algorithm is represented by Table 5-1. The information is drawn as drawn from the last five years for which this course has been offered. The algorithm itself was designed at the end of spring semester 2004*.

Date	Concept development	OTA design*	Advanced design	Projects
2003	6.5 wk	5 wk	1.5 wk	1.5 wk
2004	6.0 wk	5.5wk*	2.0 wk	1.5 wk
2005	6.0 wk	4.5wk	2.5 wk	1.5 wk
2006	6.5 wk	4.0wk	2.5 wk	1.5 wk
2007	6.0 wk	3.5wk	3.5wk	2.0 wk

Table 4-1: Measure of the impact of the algorithm on Analog IC design course. The schedule is a nominal 15 weeks. The data is taken from end semester class schedules as were readjusted during the progress of the course, (Spring semester deployment)

The advantage of the extra efficiency in addressing the OTA is that there is more time for the advanced design segment and extra presentation time for the projects (two) called for by the class schedule.

The OTA algorithm described by section IV is goal-oriented. It makes heavy use of simulation, as is essential to small-geometry devices, but does not lose sight of the analytical design process that is the usual basis for OTA design. The analytical process, which is strictly first-order, is only used to give pointers. The simulations dominate the algorithm.

It may not be evident that the algorithm accepts considerable variations, inasmuch as the design of analog circuits, OTAs in particular, does not require either an exact solution or a single solution path. In this case and example we have accomplished a good simulation roadmap that has succeeded in maximizing performance using the most economical design, with the software switch matrix as an inexpensive artifact for better flexibility and resolution of the design process.

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