Use of simulation postprocessor goal function constructs for a simple and efficient exposition of 2-terminal, 3-terminal and 4-terminal MOS device characteristics

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Abstract

Traditional device physics courses lead the student and professor through a maze of physics and mathematics that often displace the device from its principal purpose, that of a circuit component. For small geometry devices the fields can be very intense and so can the engineers that try to navigate the model descriptors without a good roadmap. The great majority of VLSI design engineers have little or no grasp of the physics behind the device, and in many instances, circuit designers tend to fly blind because the model descriptors on which they rely are only envisioned as a black art.

However a natural vehicle exists for instruction in semiconductor device physics that is seldom used by the textbook resources and device theorists. The overlooked vehicle is the circuit simulation utility. But it is designed for use as a circuit simulation platform, not as a device descriptor. Via parameterization techniques and a framework of ideal elements, a number of very effective constructs have been developed under a course taught at MSU that addresses and explains semiconductor device physics, even when the underlying physical model is not well known. These constructs can also address and parameterize circuit macros, and as such, also become of collateral value as a circuit design tool.

As result of the evolution of simulation tools, simulation postprocessors usually now include goal function options that lend considerable versatility to both the circuit designer and the instructor of circuit designers. This paper identifies particular goal functions that are of considerable merit for the exposition of the MOS device, and the necessary circuit constructs to represent it in terms of 2-terminal, 3-terminal, and four-terminal device constructs and the underlying physical expositions that are verified by the simulations. The student version of ORCAD/pSPICE, which is the most common classroom circuit simulation platform, is the vehicle that is used as the semiconductor device descriptor for the MSU course in semiconductor devices.

I. Introduction and background

Design of modern circuit electronics is defined by a cycle for which circuit concepts are confirmed and assessed by means of a circuit simulation utility. The most common platform for circuit simulation in the academic environment is one of the several versions of the SPICE [1-3] utility, since its emphasis is integrated circuit design. As the circuit process has matured this utility has evolved into a friendly and flexible resource that has found a role in almost every part of the electrical and computer engineering curriculum.

As is true for this and other circuit analysis software, SPICE is constructed as a linear algebra that will assess a circuit with n nodes as an $n \times n$ matrix, with any non-linear elements within the circuit tasked by a Newton-Rhapson iteration and various sparse matrix techniques [4]. The principal mathematical requirement of the non-linear components is that device models used by the software be uniformly continuous, and since this construct does allow piecewise constructs, the results can be mildly non-physical.

The mathematics for device models is developed from semiconductor physics. Generally the device physics dominates the classroom instruction and application to device simulation is either an assumption or is passed along to other parts of the curriculum. Device physics usually demands a great deal of overhead and can dwell on anything from thermodynamics to field theory. And the devices themselves can range from two-terminal non-linear resistances to four-terminal transistors. Use of SPICE to illustrate performance characteristics of devices are not uncommon in the circuits courses, but are uncommon in the semiconductor devices courses.

Most of the instructional framework and time commitment given to semiconductor devices is submerged in the mathematical expositions necessary to describe the physics of the device [5]. This is particularly true for small-dimension devices where high-field effects [6-9] predominate and change the nature of the device performance. Most of the literature is dedicated to semi-empirical physics assessments and use of special test vehicles to evaluate the effects in question. The requirement then falls upon the instructional process to either commit to relatively selective literature analyses or rely on the first-order physics to define the operation aspects of the semiconductor devices in question. Higher-order device models must accommodate so many effects that the analytical overhead becomes enormous, and an exposition can overwhelm both the semester time frame and the students, and often leaves the engineers in a subtended role for which they do not have a high confidence factor in their semiconductor device foundations.

In this paper, the use of the circuit simulator and its platform of models and embedded formulations is applied and endorsed in lieu of the extended analysis overhead, with only a bare minimum of mathematical exposition. The evolution of circuit simulators, particularly those in the public domain, have given the instructor a very flexible and extensive platform that facilitates this process, and considerably reduces the overhead with a considerable gain in coverage and throughput.

II. Simulation Artifacts

The simulation platform affords a reasonable accurate vehicle for examination and assessment of device physics, since the mathematical models that are used in the classroom are embedded. The simulation platform, however, is geared toward network facts, such as node voltages and branch currents more than it is for characterization of the embedded devices.

However, device features can be extracted from the electrical data field by means of postprocessor functions, judiciously applied to artifacts called 'goal functions', which can span simulations for which a device parameter is varied. Typically, goal functions yield information about maxima, slopes, and device measures, such as capacitance as a function of a designated parameter. For example the C(V) relationship as a realizable plot artifact is accomplished by an unusual construct provided by the pSPICE postprocessor, of the form:

YatX(,)

Which can be applied to a simulation construct of the form

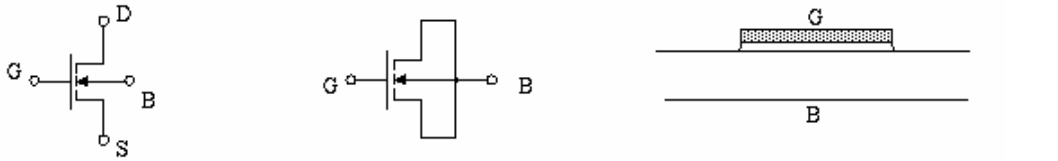
$$C(V) = imag\,(I(\omega)/V(\omega))/(2\pi f) \qquad (2.1)$$

And is illustrated in the several C(V) examples identified in the later sections.

Otherwise the postprocessor can extract parametric relationships for any of the conduction characteristics as a function of the various device parameters embedded in the model parameter file. And where needed the data can be transported to other platforms, such as spreadsheet forms [12], for assessment and curve-fitting.

III. Two-terminal devices: The MOS junction

The only MOS device that exists within the pSPICE schematics library is the 4-terminal MOS transistor as indicated by figure 3.1(a). It can be reconfigured as a two-terminal device as indicated by figure 3.1(b), with effective construct as indicated by figure 3.1(c).



(a) 4-terminal library part (b) 2-terminal equivalent config (c) 2-terminal physical cross-section

Figure 3.1: Reconfiguration of the 4-terminal MOSFET part as a 2-terminal MOS junction.

In the lecture deployment of the MOS device family, the two-terminal analysis is essential to interpretation of such concepts as threshold and body effect. The interpretation is facilitated by the fact that the characteristic Si-gate MOS junction is not unlike a pn junction, except that there is an oxide layer that lies between the *p*and the *n* layers, as represented by figure 3.2.

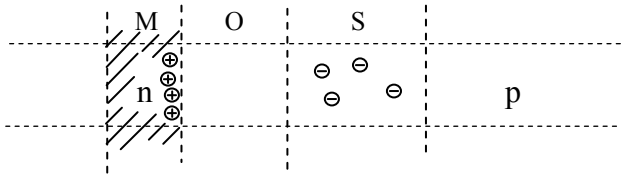


Figure 3.2 Charge distributions across the silicon-gate MOS junction

The (silicon MOS junction is non-conductive since one of its layers is SiO_2. Therefore the only relevant physics would be defined by a C(V) plot as represented by figure 3.3(a).

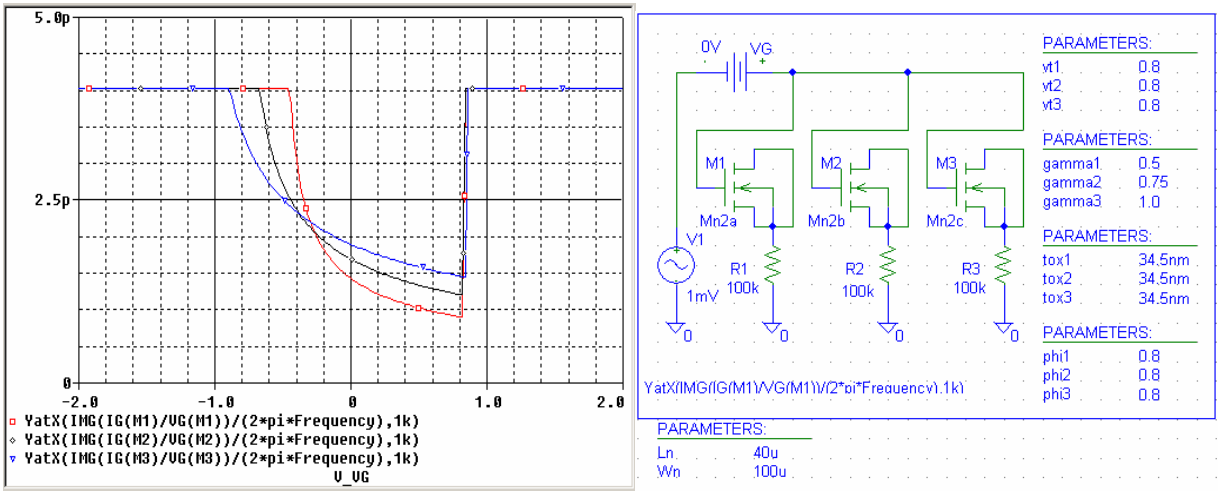


Figure 3.3(a) MOS junction C(V) plots using level-2 (= physical model[1]) analysis.
Figure 3.3(b) Circuit construct using MOS transistor and parametric mode to create plot family.

Figure 3.3(b) indicates the technique of exporting key parameters from the model file into the parametric declaration, for which each transistor can then represent a behavioral family of curve traces. In this case the construct discloses the behavior of *C(V)* as a function of the level-2 parameter γ (gamma), otherwise know as the 'body effect'. Otherwise the schematics construct is not unlike that used for the pn junction, as may be seen by comparison to figure 2.3(a).

But it should be evident from figure 3.3(a) that the physical model is less than realistic, since the physical device would not have the piecewise form indicated. The mathematics representing figure 3.3(a), which is the first-order E-field model of the MOS junction, is of the form:

$$C(V) = C_{OX} \Big/ \sqrt{1 + \frac{4}{\gamma^2}\left(V_G - V_{FB} - V_B\right)} \qquad (3.1)$$

and has breakpoints at V_G-V_{FB}-V_B = *0* and at V_G=V_{TH}, as indicated by figure 3.3(a). For this device the threshold voltage V_{TH} is set to 0.8V, which is readily evident in figure 3.3(a). The substrate bias is set to V_B = *0*. The behavior indicated by figure 3.3(a) is representative of the classical physics descriptions used by the level-2 model.

If we graduate from the level-2 model to the level-7 model (level 49 in HSPICE), a more comprehensive model of the MOS device, as well as being a short-channel model, then we have a two-terminal C(V) behavior that is considerably more realistic, as represented by figure 3.4.

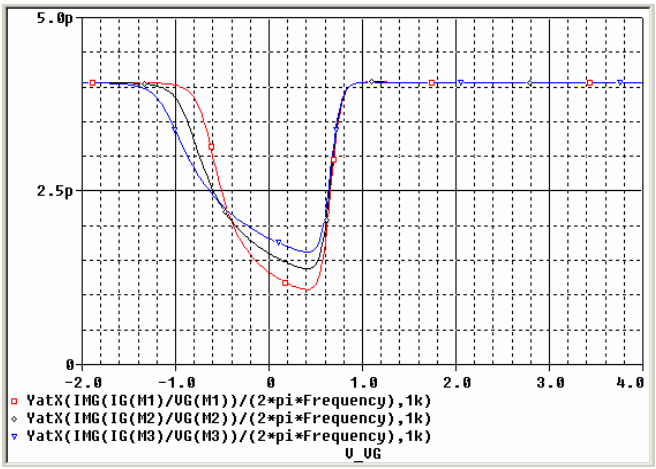


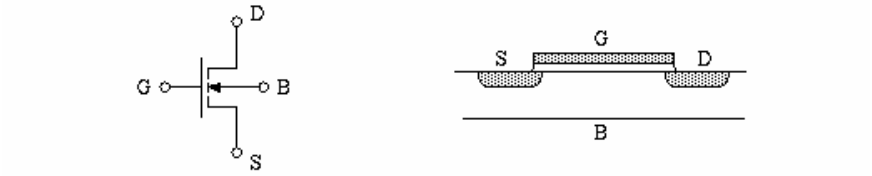
Figure 3.4 C(V) behavior of 2-terminal MOS device for level-7 model[3]. Device size is chosen as W/L = 100µm/40µm and t_{OX} = 34.5 nm in order to avoid small-geometry effects.

The same schematic as was used in figure 3.3 was applied, the only change being in the device model that is invoked. The behavior represented by the level-7 result is consistent with the transcendental analysis[10] of the MOS junction using thermodynamics and E-field analysis.

IV. MOS device as a 3- and 4- terminal component

As indicated by the library component, the MOS device is a 4-terminal construct, as emphasized by figure 4.1. Typically, its device model lends itself best to an interpretation for

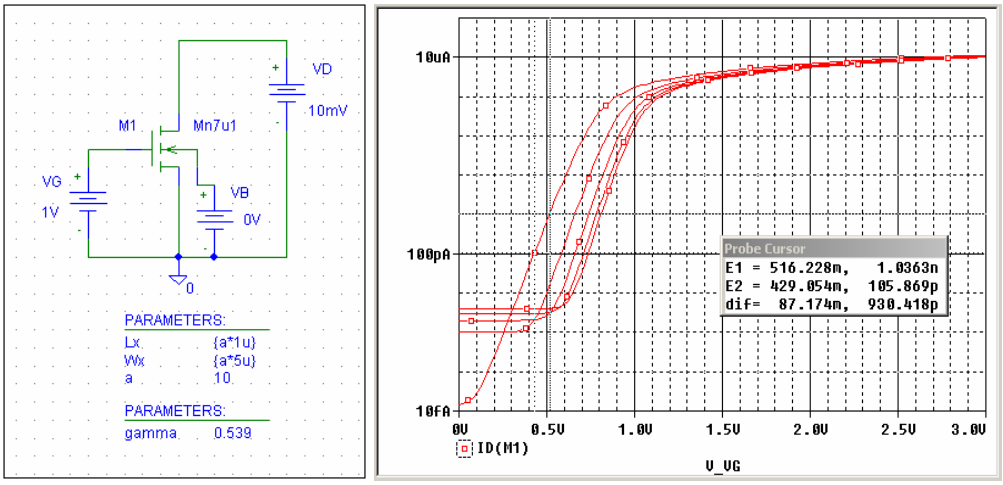
which the gate-source-body terminals are used to define threshold and operation of the device at low transport fields and the four-terminal model is used to define high-field effects.



(a) 4-terminal schematic symbol (d) physical cross-section

Figure 4.1. 4-terminal MOS device (transistor)

The low-field effects can be identified very easily by means of $I(V_{GS})$ characteristics developed by pSPICE, as represented by figure 4.2, with V_{DS} = 10 mV and back-bias V_{BS} stepped to identify body effects. The MOS device is developed in terms of the more advanced model (level-7) for the more realistic behavior. With larger device sizes, as selected, the small-geometry effects are inconsequential and the behavior indicated by figure 4.2 should be adaptable to most of the first-order physical explanations.



4.2(a) Test schematic 4.2(b) $I(V_{GS})$ for V_{DS} = 10 mV

Figure 4.2 Low-field subthreshold characteristics, 4-terminal MOS transistor

The behavior of the channel current of the MOSFET for $V_{GS} < V_{TH}$ is not unlike that of conventional *pn* junction behavior, except that the emission coefficient is identified in terms of the sub-threshold slope factor. For cursor measurements shown, the value of this factor is:

$$\text{nfactor} = 87.17/(25.67*2.43) = 1.392 \qquad (4.1)$$

Which for back-gate bias VBS = 0. The result is consistent with the level-2 device theory [1,5]

$$\frac{1}{nfactor} = \frac{1}{1+\alpha}\left[1 - \frac{1}{\sqrt{1+\left(4/\gamma^2\right)\left(V_{GB}-V_{FB}\right)\left(1+\alpha\right)}}\right] \qquad (4.2)$$

which, for $\gamma = 0.539$ as assumed by 4.2(a), and $\alpha = 0$, $V_{GB} = 0.473$ (from plot 4.2(b)) and $V_{FB} = -0.351$, yields an *nfactor* of 1.398.

As one further illustration of the power of the simulation to define and explain the physical behavior of the MOS devices, we can use pSPICE to prosecute the C(V) behavior for the 4-terminal MOS device, much in the same way as it was used to assess the C(V) behavior for the 2-terminal construct. The 4-terminal MOS device no longer can be defined as a two-terminal capacitance but must be defined as a 4-terminal capacitance matrix for which the capacitances are of the form:

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \qquad (4.3)$$

for which indices {i,j} relate to the 4 terminals {G,D,S,B} of the MOS device as indicated by figure 4.1. The four-terminal capacitance matrix is a relatively complex construct, but for the channel-charge layer it can be represented, to first order, by the Meyer model[11] for which the capacitance at the gate terminal (G) is:

$$C_{GG} = \frac{2}{3}C_O\frac{a^2+4a+1}{\left(1+a\right)^2} \qquad (4.4a)$$

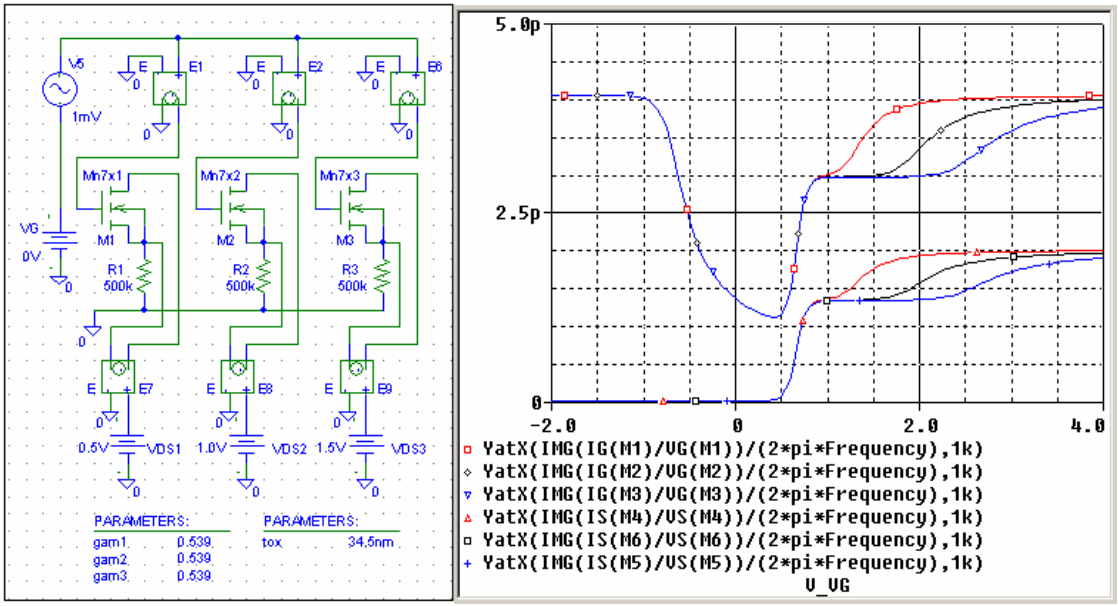
and at the source terminal (S), is:

$$C_{SS} = \frac{2}{3}C_O\frac{8a^2+9a+3}{\left(1+a\right)^3} \qquad (4.4b)$$

There are but 2 of the 16 terms in the MOS capacitance matrix. Both can be represented by simulation analysis. In equations (4.4a) and (4.4b), $C_O = C_{OX}\,x\,(W x L)$ is the area capacitance of the MOS device, and

$$a = \frac{V_{GS}-V_{DS}-V_{TH}}{V_{GS}-V_{TH}} \qquad (4.5)$$

for which a -> 1 as V_{DS} -> 0, and a -> 0 for V_{DS} ->large. These capacitances can be implemented in pSPICE in the same manner as was accomplished by figure 3.3, using the construct identified by equation (2.3):



4.3(a) Test schematic (for C_{GG}) 4.3(b) C_{GG} and C_{SS} capacitance matrix terms

Figure 4.3: Capacitance matrix terms for the 4-terminal MOS device

Note that the set of curves for the gate capacitance as represented by matrix term C_{GG} are represented by the pSPICE construct

YatX(IMG(IG(M1)/VG(M1))/(2*pi*Frequency),1k) (4.6)

and are an extension of the two-terminal MOS device *C(V)* response indicated by figure 3.4. The $C_{GG}(V)$ behavior is accomplished in pSPICE via a piecewise construct that otherwise would be a time-consuming and tedious class exercise.

Display of the behavior represented by figure 4.3 is more than just convenient. Measurement of MOSFET capacitances is itself a non-trivial process, since the devices are micron-sized and the entire measurement apparatus, to include on-chip interconnect patterns, must be compensated before C(V) measurements can be believed. The power of the simulator is emphatic and friendly for the classroom development of the complexities of this device, without the incipient overhead that is necessary from the mathematics, physics, and measurement environment.

V. Conclusions

The constructs that have been identified in the preceding sections are but a few of many options, since the capability of the simulation software to identify the effect on I(V) and C(V) behavior of working devices is extensive and has reached a point of viability that makes it a

classroom tool that can be used to accomplish much more than a proof test for circuits and circuit design. Most of the capabilities of the simulator that have provided this enhancement are a consequence of upgrades in the post-processor. These upgrades now allow the simulation data to be manipulated in ways that are much more than a simple electrical analysis, and extend well beyond the focus of circuit proof and performance analysis. The device models in pSPICE have evolved over time to the point that they now represent actual devices to a higher degree of accuracy than the simplified models ordinarily identified in the classroom or laboratory. And this paper has found a practical means to investigate aspects of device behavior from simulation that is more accurate and less complicated to implement than simple theories or laboratory measurements.

The capability to analyze devices is a demand item, since circuits of micron and sub-micron dimensions are difficult to assess both before and after the fact, since the devices are only assessed as part of a test vehicle, which leaves the engineer at the mercy of the complex relationships developed thereto. For example the level-49, BSIM3V3 model[3], as accepted and continuous form simulation model as it may be, is an engineer's nightmare, since the model requires 108 parameters and a mathematics that is nearly impenetrable without a large investment of time and detailing. It is a model that is predicated as a quadratic approximation, which provides a baseline simplicity but requires a serious number of patches in order to assure continuity over all regimes of operation. The BSIM3V3 model has been upgraded and appended many times since its inception, and has accumulated many small-geometry and short-channel effects, some of which are more than a little arcane, and makes it an enormous task to unravel the relationships embedded within.

Fortunately the advances in the postprocessor software have become of considerable value in devolving these effects and avoiding the details necessary to explain and interpret the relationships. The constructs that have been illustrated for the pSPICE simulator are excellent for the classroom environment and have proven to be of considerable value to many of the higher-order effects without being drowned by the physics/mathematics details and overhead, and this has been proven of high value and high throughput for the segment of the academic community concerned with device physics. It has made the use of descriptive analyses practical, viable and succinct.

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