Using Commercial EDA Software in Computer Engineering

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Christopher Newport University (CNU) has standardized on the Cadence EDA (Electronic Design Automation) tools for its new Computer Engineering curriculum. This choice was based on our experiences with EDA tools and carries with it both advantages and disadvantages. This paper will discuss many of the issues associated with using commercial tools in the classroom and also describe how we are using the Cadence tools at CNU.

Pros and Cons of Commercial EDA Tools

Some of the Pros and Cons of commercial EDA tools are summarized in Table 1.

Pros	Cons
Real World Exposure	Steep Learning Curve
Engineering Quality Products	Requires High End Workstation Environment
Common User Interface for all Tools	Requires Systems Administration Support
Annual Upgrades	Annual Fee
Hotline Product Support Available	
Training Support	

Table 1: Pros and Cons of Commercial EDA Tools

Problems with commercial EDA tools typically fall into two categories; those associated with systems administration and those associated with the learning curve the student encounters. Administrative problems can be solved with appropriate levels of funding. To successfully use commercial tools like the Cadence products, a high-end workstation laboratory with enough seats to support engineering courses is required. Although it is possible to run these Cadence tools on a Sparc II, it is recommended that as least a Sparc 5 is used with 32MB of memory. The laboratory will require systems administration for maintenance and software upgrades. Cadence provides CNU with regular upgrades as part of our annual agreement which costs $5,000/year. Users should plan regular upgrades to keep current with EDA technology, but be careful not to upgrade during the semester in case something goes wrong.

The learning curve problem can be solved by spreading out the use of EDA tools throughout the curriculum. We expose students to schematic capture and simple analog and digital simulations at the sophomore level. Advance use of the tools occurs in junior and senior level courses. This incremental approach reduces student frustrations, but requires professors teaching different courses to cooperate in the use of EDA tools. A benefit of using the tools in multiple courses is the reinforcement the students get. Since the design framework is common for all the tools, exposure to the framework occurs over and over again as students take courses. Students do not have to learn a completely new system for each class, for example the same schematic capture system is used for both the analog and digital design courses.

The major advantage of using commercial EDA tools in the classroom is the real world experience students obtain. Mastering a sophisticated commercial tools set also seems to aid students in finding employment upon graduation. Using engineering quality software products in classroom and for laboratory projects builds an experience base for the student which is reflected in student maturity in problem solving.

EDA Tool throughout the Curriculum

Our approach of integrating EDA tools throughout the computer engineering curriculum at CNU encompassed six courses, but can be easily extended to include even more. Tools can be roughly classified as digital or analog although Cadence supports mixed mode tools (which we have not used) and physical design tools (which we hope to incorporate in the future) as well.

Analog Tools

In our traditional two semester calculus based electric circuits courses we have started using the schematic capture and an analog simulator. This allows for graphical entry of analog circuits and simulation with engines like cdsSpice or Spectre. Graphical output is available for displaying simulation results. Figure 1 and Figure 2 show a typical simple circuit with its corresponding output. These tools also supports a waveform calculator which allows the student to manipulate the output waveforms by integration, differentiation and many other functions. These tools can be introduced in the classroom through demonstration. It is useful to show the effects of sweeping circuit parameters across a range and simultaneously viewing the multiple output waveforms. The tool can also be used in the laboratory side by side with hardwired circuits to compare predicted and actual results.

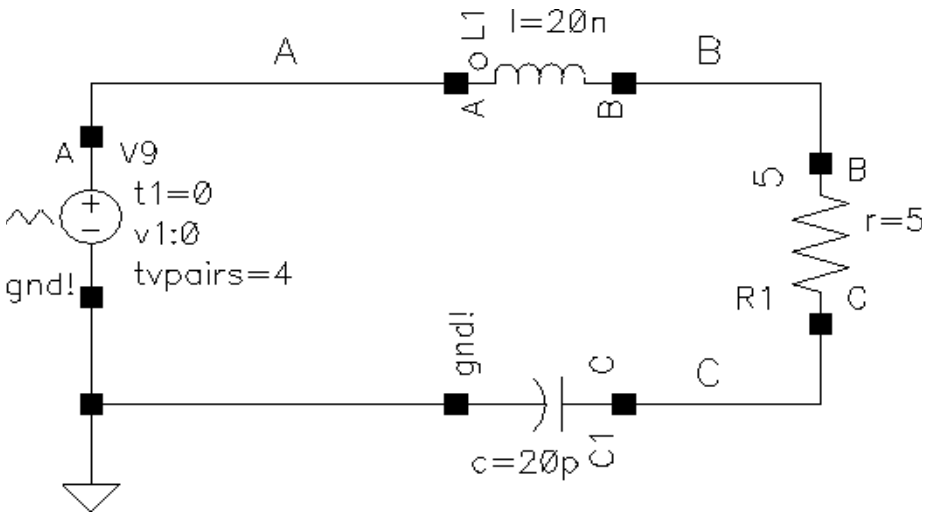

Figure 1: Analog Circuit

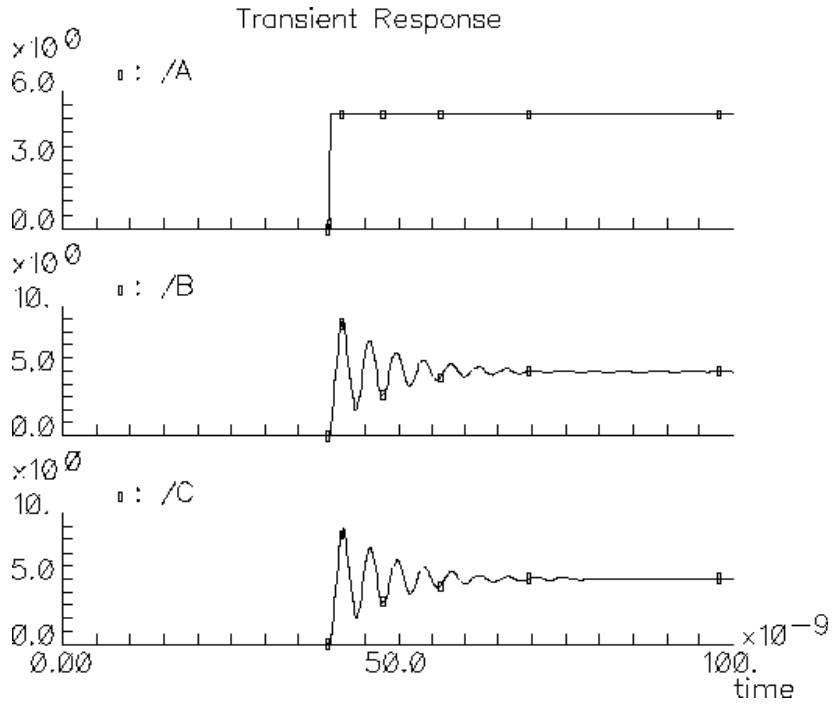

Figure 2: Analog Simulation Output

Digital Tools

The digital tools are first introduced in our introductory Digital Logic Design class. Schematic capture and digital logic simulation are performed. Once again, the design framework is common for all the tools and therefore the same schematic capture tool used in the circuits classes is used in the digital course. In the class we attempt to simply expose the students to the tools with just one or two simple designs. Once again circuit entry and output displays are graphical. The simulator used is Verilog-XL, although at this level it is transparent to the user. Accurately modeled TTL design libraries are available as well as are many others. Figure 3 and Figure 4 show a digital circuit and its corresponding simulation output.

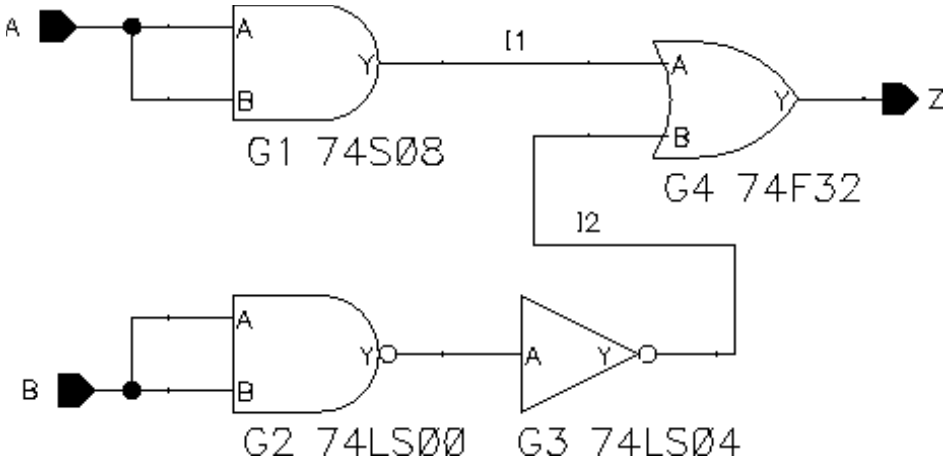

Figure 3: Digital Circuit

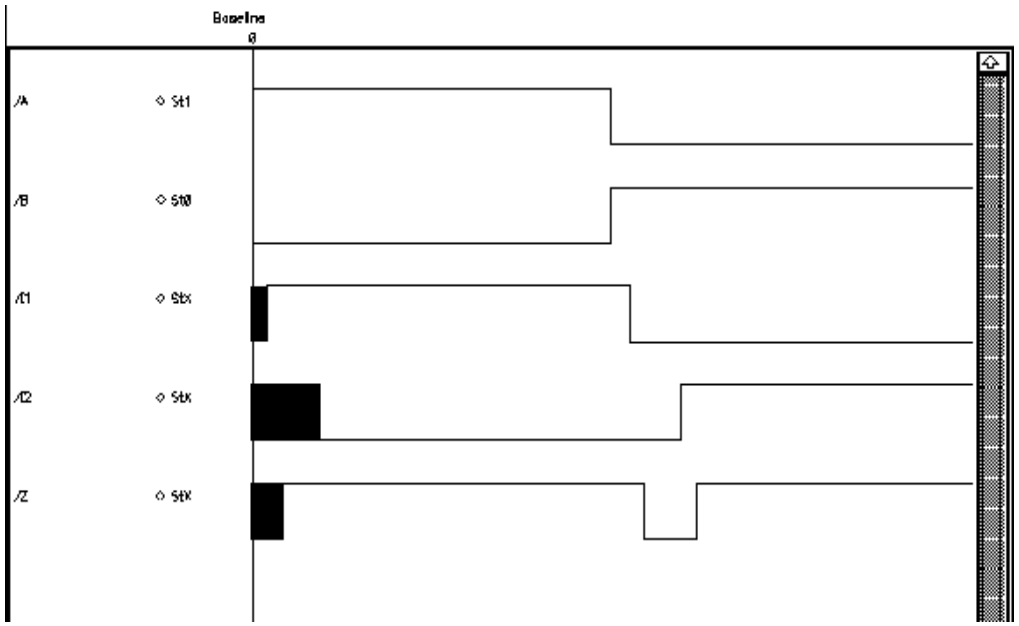

Figure 4: Digital Simulation Output

During the second semester of digital design/computer organization students begin to explore more features of the Cadence tools. The hierarchical features of the schematic capture are introduced for functional design decomposition. A few more features of Verilog are covered including exposure to a state machine description that is synthesized to a schematic. Simulated designs are implemented in PLDs and tested in the laboratory. Cadence provides several tools for programmable logic device support. At the end of this semester student confidence in the design environment is evident.

Computer Architecture is the next course that utilizes EDA tools. CNU uses the Hennessy and Patternson text for computer architecture that cites the DLX processor for pipeline examples. In this class, students modify a Verilog simulation model for the DLX. The DLX is decomposed into stages that are graphically represented as boxes connected by wires and busses. Behind each box is a Verilog model. After an overview of Verilog, students are required to modify the design to handle data dependencies with pipeline stalls and data forwarding. These exercises introduce system level modeling using a hardware description language (HDL). We use Verilog because of its dominance in VSLI design and its similarity to C and C++. C++ is the language taught in our lower level language courses and much of the Verilog syntax is similar.

In CNU's senior computer engineering laboratory course, the Cadence tools are used for the design, simulation and implementation of a Xilinx FPGA based design. The Cadence/Xilinx flow is shown in Figure 5. These projects reinforce the simulation environment from previous courses and extend the design process to FPGAs. Standard Xilinx prototype cards can be used for student designs or custom FPGA based designs can be implemented.

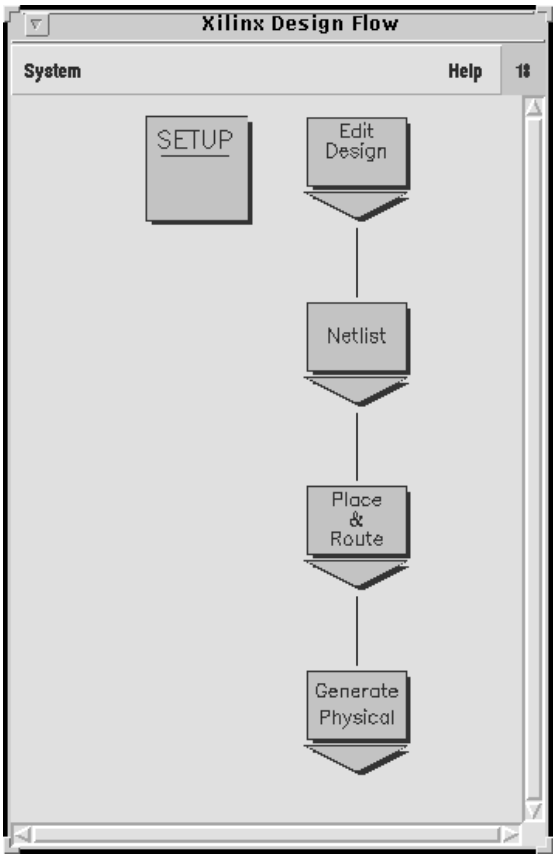

Figure 5: FPGA Flow

Additional Tools and Future Direction

Many additional EDA tools are available through Cadence which have not been discussed. Table 2 lists some of the additional tools that may be useful in engineering programs. We have had experience with the standard cell and custom ASIC tools and have successfully fabricated devices using the MOSIS 0.8 micron CMOS process. In the future we plan to add a VLSI design course which will focus on some of the physical design tools. All the front end tools remain the same as in existing courses. Another future project is to create a board level simulation model for students to use in a microprocessor class. Verilog models exist for many microprocessors. Third party models would most likely have to be purchased to complete this design, but a project like this would expose students to board level interfacing concerns.

EDA Tool	Use
Allegro	PCB Layout
Allegro MCM, SigNoise, Thermax	MCM Tool
Cell Ensemble, Layout Editor	Standard Cell / Custom Layout
Dracula	Design Verification DRC, LVS, ERC
Verifault	Fault Coverage

Table 2: Additional Cadence Tools

Conclusions

CNU has successfully integrated commercial EDA tools into it computer engineering curriculum. To maximize the benefits of commercial EDA tools and to minimize the disadvantages we feel an integrated approach is best. Using the tools in several courses and incrementally exposing the students to new features is important to conquer the learning curve of complex tool set. We also caution users to be aware of the administrative and budgeting concerns associated with running a high-end workstation laboratory. Commercial tools in the classroom can work well to the benefit of the student but the effective use of these tools requires careful planning across the curriculum.