

Using the Rasterizing Capability of the AMD 29205 Microprocessor

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Abstract

The AMD 29205 32-bit RISC microprocessor includes many input/output features that can form the basis for lab experiments in academic settings. One of these features is the rasterizing shift register built into the processor. This feature allows generation of raster images, as in CRT displays, or capture of images supplied externally in raster form as from image scanners. This paper details the techniques used in a microprocessor laboratory to generate a CRT image of both text and graphics using the rasterizing hardware built into the AMD 29205 processor.

Background

This paper is an extension of a paper presented previously at the 1995 ASEE annual conference¹ that detailed the techniques for designing a microprocessor lab around the 29205 processor. The lab station described in that paper included both the SA-29205 demonstration board for the processor and a separate terminal for interaction with a host computer. The lab station in that microprocessor laboratory is evolving away from the need for the separate terminal by using the processing power available in the 29205 itself to perform the terminal functions of keyboard input and CRT screen output. In order to complete that transformation in the lab station, generation of a text and graphics image on a standard CRT must be accomplished.

The SA-29205 demonstration board provides a generous amount of memory on the board to support bit-mapped graphics, and that facility is used in the techniques described here to generate the rasterized image. Many other features of the 29205 processor, such as the internal Direct Memory Access (DMA) capabilities and the simple support for external peripherals added to the processor, are used extensively. Using the rasterizing feature of the AMD 29205 not only demonstrates that particular capability of the processor, but also provides a good example of the overall capabilities that are available in a lab based on the 29205.

Detailed below are the techniques in both hardware and software that have been used successfully to generate a raster image for a standard CRT display using the rasterizing capability of the AMD 29205 microprocessor. Also included are some experiments assigned to students using this interface, and some ideas for future applications of this improved lab station.

Hardware

The hardware in the 29205 microprocessor that supports raster image generation is centered around a 32-bit shift register. Bits in this shift register are shifted out one end or the other,

determined by a control bit, to become the video signal that controls the electron beam in the CRT display. The shift register is double buffered using a 32-bit "Video Data Holding Register" (VDATA) to reduce the overhead imposed on the software or hardware that supplies data to the system. Many aspects of the operation of this shift register are programmable using the contents of the "Video Control Register" (VCT) in the 29205.

One characteristic that must be programmed in VCT is the clock rate at which the video shift register is shifted. This is derived from an external clock input, which in this case, is connected to the 29205's main timing reference, MEMCLK, that runs at 16 MHz. This external reference, 16 MHz, can be divided internally by any factor from 1 to 16 to produce the internal shift register clock, which becomes the bit rate for the video data. The factor chosen determines the resolution of the display along a scanline of the CRT. In a standard CRT display, scanlines are generated with a frequency of 15 KHz to 16 KHz, which yields about 65 μ sec for each scanline. Generally 10% to 20% of this time is not available due to overscan of the monitor and required retrace time, so typically one can count on about 50 μ sec of usable time on each scanline for image generation. With the maximum resolution available, using a clock division factor of 1, the shift register shifts at 16 MHz, producing about 800 pixels of image resolution along a scanline in those 50 μ sec.. The number of scanlines across the screen determines the resolution in the direction orthogonal to the scanlines. This number is determined by the ratio of scanline frequency to the frequency at which the entire screen is refreshed, generally near 60 Hz. This ratio leads to about 250 to 260 scanlines. Again, 10% to 20% of these scanlines are unusable for image generation due to overscan of the CRT and required retrace time for the electron beam, so image resolution in the direction orthogonal to the scanlines is only about 230 to 240 pixels. Since a standard CRT screen has an aspect ration of about 4:3, with the long dimension parallel to the scanlines, the resolution along the scanline was chosen to be about 400 pixels, using a clock division factor of 2, to yield pixels that are approximately square in the image while still maintaining reasonably high resolution along the scanlines.

Another aspect of image generation that must be established is the synchronization of the pixels coming out of the shift register with the scan of the CRT screen itself. This is accomplished with two signals, "Line Sync" (LSYNC) and "Page Sync" (PSYNC). LSYNC is always an input to the 29205 processor, and determines when a scanline begins on the CRT screen. PSYNC can be either generated by the processor or supplied externally as determined by programming in VCT. In the case discussed here, PSYNC is supplied to the 29205 by external hardware. These two signals also run with the video signal to the CRT so that in addition to telling the 29205 when a scanline and a page start, they also control the scan of the CRT so that the processor and the CRT operations are synchronized. via those signals. The two signals are generated by an external string of flip flops that divide the 16 MHz MEMCLK signal by factors of two each. The 16 MHz MEMCLK signal is first divided by 1024, using ten flip flops, to produce 15625 Hz, which is used for the LSYNC signal. LSYNC is then further divided by 256, using eight more flip flops, to produce about 61 Hz, which is used for PSYNC. The image on the screen uses twelve 32-bit words of data per scanline, for 384 pixels along the

scanline, and 224 scanlines. The screen is oriented with the long dimension vertically, so that scanlines run from the bottom of the screen to the top.

Centering the image on the screen is accomplished with two other registers inside the 29205. The "Top Margin Register" records the number of scanlines at the beginning of a page to skip before starting to put out image data, to allow centering the image along the short dimension of the screen. The "Side Margin Register" records the number of pixel positions to skip at the beginning of each scanline, to center the image along the long dimension of the screen. This second register also records the number of pixels of image data to be output on each scanline, which determines how much of each scanline actually is used to show image data.

Finally, the VCT register contains control bits that allow software to configure the rasterizing hardware to match requirements of the particular set up. Bits are available to establish the direction in which the shift register shifts, and to conditionally invert LSYNC, PSYNC, and the video data itself to match the needs of the CRT in the system, along with other details. In short, the rasterizing hardware in the 29205 provides a very flexible and capable system that performs most of the work in generating a raster CRT image.

Software

Because of the efficient support for raster displays provided by the 29205 hardware, the software required to support the display function is relatively easy. The main task of the software is to copy pixels to VDATA quickly enough to keep up with the scan of the CRT in producing the image. With the parameters identified above of 224 scanlines with twelve 32-bit words on each scanline, a total of 10752 bytes of memory is required to store a bitmap of the screen image. On the 29205 system in this laboratory, memory addresses between 4007d600 and 4007ffff hexadecimal are used for this purpose. This is only a small fraction of the half megabyte of RAM that is supplied on the SA-29205 demonstration board used in the lab station.

Getting the information from RAM to the VDATA holding register quickly enough is the only problem to address here. To produce an image with the resolution specified above, twelve 32-bit words must be copied to VDATA every 50 μ sec, or about 4 μ sec per word. Although software polling is possible to determine when the VDATA needs to be refilled, such an approach cannot keep up with the required data rate. The video hardware also supports interrupt generation whenever VDATA empties into the shift register, but an interrupt every 4 μ sec is too much to demand also. The only option for supplying data to the video system fast enough is Direct Memory Access (DMA). Fortunately, the 29205 includes two internal DMA channels, either of which can be used to supply data to VDATA on demand. By setting up a DMA transfer to copy words of RAM starting at address 4007d600 to the video system, and ending with the last word in the bitmap section of memory, the entire process of copying the bitmap memory to VDATA for image generation proceeds completely behind the scenes and out of sight of the programmer. The DMA channel causes an interrupt at the end of every screenful of information, which serves to reinitialize the DMA transfer for the next screenful.

With that system in place, all that is required to produce an image of any sort is just to modify memory locations between 4007d600 and 4007ffff to create the pixel pattern required for the desired image.

Experiments

Many different experiments are possible using the bitmapped CRT display controlled by the rasterizing hardware in the 29205 processor as described above. These experiments range from simple graphics images to full text displays. All that is required is to turn on the right pixels in the bitmap section of the memory. Software can produce lines, filled areas, or text characters by merely turning on the right bits.

Simple graphics displays are probably the easiest applications with which to work. Students in classes using this lab have successfully designed and implemented graphics-based games such as a simple "Pong" game and a screen drawing program that simulates the "Etch-a-Sketch" toy. These games have been used as lab exercises in the last week of a ten-week quarter during which students have learned to use the 29205 processor and its features.

Applications that require text display need to use a character generator table in memory that stores the bit patterns for the various character fonts. Printing a character on the screen is just a matter of copying the bits representing the character to the proper pixels in the bitmap area of memory. Students have written programs to show multidigit numeric displays on the CRT screen, and a full text display to implement the output side of a terminal emulation program is under development.

Given the large amount of memory available in the SA-29205 demonstration board used in the lab station, many additional applications for the bitmapped display described above are possible. Given enough time and patience, software that rivals the performance of commercial game units is achievable.

Summary

In summary, the rasterizing hardware included on the AMD 29205 microprocessor makes possible a raster video display using bitmapped graphics on a standard CRT monitor as described in this paper. The hardware included in the processor, along with minimal external hardware support for synchronizing the 29205 software with the scan of the monitor, makes software development to support the display easy. The resulting display can be used to produce a wide variety of graphics or text images, limited only by the imagination and patience of the programmer. Using the rasterizing capabilities of the 29205 processor is a successful and rewarding experience.

References

1. Carroll, C. R., "A Microprocessor Laboratory Based on the AMD 29205 32-bit RISC Processor," *1995 ASEE Annual Conference Proceedings*, Anaheim, CA (1995).

Biography

CHRISTOPHER R. CARROLL received a Bachelor of Engineering Science degree from Georgia Tech, and M.S. and Ph.D. degrees from Caltech. After serving in the Electrical Engineering department at Duke University, he is now Associate Professor and Assistant Head of Electrical and Computer Engineering at the University of Minnesota Duluth. His interests include special-purpose digital systems, VLSI, and microprocessor applications.