Voltage and current loop controlled three-stage three-port solid state transformer

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Abstract:

Future of smart grids is mostly dependent on the latest advances in research on Voltage Source Inverter (VSI). The VSI mainly consists of power electronic devices i.e. IGBT, MOSFET, etc. with high switching frequency operation. High power converters are now being considered for the transmission and distribution of power systems such as in high voltage DC (HVDC) transmission, flexible AC transmission systems (FACTs), and STATCOM, etc. Along with these applications, solid-state transformer (SST) is getting much attention for the high-power transmission and distribution systems. SST facilitates HVDC power transmission with reduced transformer size, low cost, and easy mobility. A three-stage three-port SST with two loop-controlled systems is presented and discussed in this paper. The concept of the converter-based transformer allows the increase in frequency that dramatically reduces the size of the transformer coil resulting in overall reduced cost and weight. A multilevel converter is used in the first stage to accommodate high voltage and divided into two port using conventional converter structure in the secondary side of the transformer. The effectiveness and correctness of the structure are validated by simulation results. We intend to incorporate the findings of this paper in projects and labs for the upper-level undergraduate power electronics class to demonstrate the relevance and significance of our research in industry so that students can gain state-of-the-art experience in the laboratory before they graduate and perhaps be encouraged to pursue advanced degrees and/or research-based positions. The power electronics-based power transformer information presented in our paper can be used to develop advanced power electronics upper-level undergraduate or introductory graduate level courses. To take full advantage in understanding and appreciating the content of the advanced power electronics course, a pre-requisite course in introduction to power electronics and control system is recommended. Our literature review on different SST structures presented in this paper will be the primary knowledge needed in understanding and design of SST model.

Introduction:

The power grid is mainly divided into three main sections, power generation, transmission, and distribution. The power generation consists of a power plant that produces power from renewable or non-renewable energy sources at low to medium voltage. This voltage is then increased in order to transmit the power from the generation site to the distribution site. At the distribution level, the voltage is again reduced for the consumers. Power transformer, in this case, plays a very important role to step up and step down the voltage. There have been many advancements in the conventional transformer, mainly magnetic coils, materials, cooling system, manufacturing process etc., but the advancements of the transformer structure and functions are first proposed in [1] where power electronics technology is combined with the power transformer. This technology allows the increase in frequency that significantly reduces the magnetic coils as well as the overall size and the cost of the transformer. However, the power converter has been

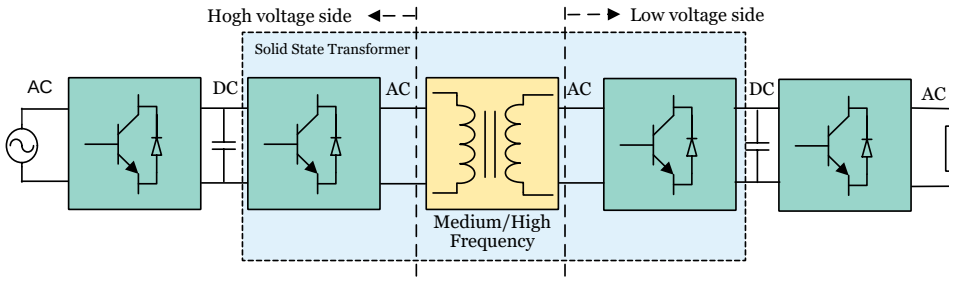


Figure 1: Basic structure of SST.

considered for medium to high voltage level applications over the past decades especially for HVDC, FACTS, STATCOM etc. The main idea of the SST is to apply high-frequency signal to the power transformer to reduce the coil size since the number of coils is inversely proportional to the frequency. The traditional 50 or 60 Hz frequency signal can be transformed with tens of kilohertz level which drastically reduce the coil size. Using a secondary converter can again lower the frequency into distribution level frequency (50/60 Hz). This total process can only be done using power converters. There has been extensive research on SST during the last decade and many topologies of SST were proposed [2]-[5]. The basic structure of the SST model is shown in Figure 1. There are many SST topologies based on the type of converter used and the application. There are many applications of SSTs such as compensation of Var and voltage sag, renewable energy source integration and bi-directional power flow. Four SSTs model is commercially developed and tested by many companies i.e. universal and flexible (UNIFLEX) [6], EPRI [7], ABB [8] and GE [9]. The UNIFLEX SST model is a multi-stage and multi-port power electronics converter designed mainly for smart grid applications. The EPRI SST topology uses the NPC configuration for the high voltage side and is designed for dc fast charging applications. GE mainly designed the SST model for substation applications with the

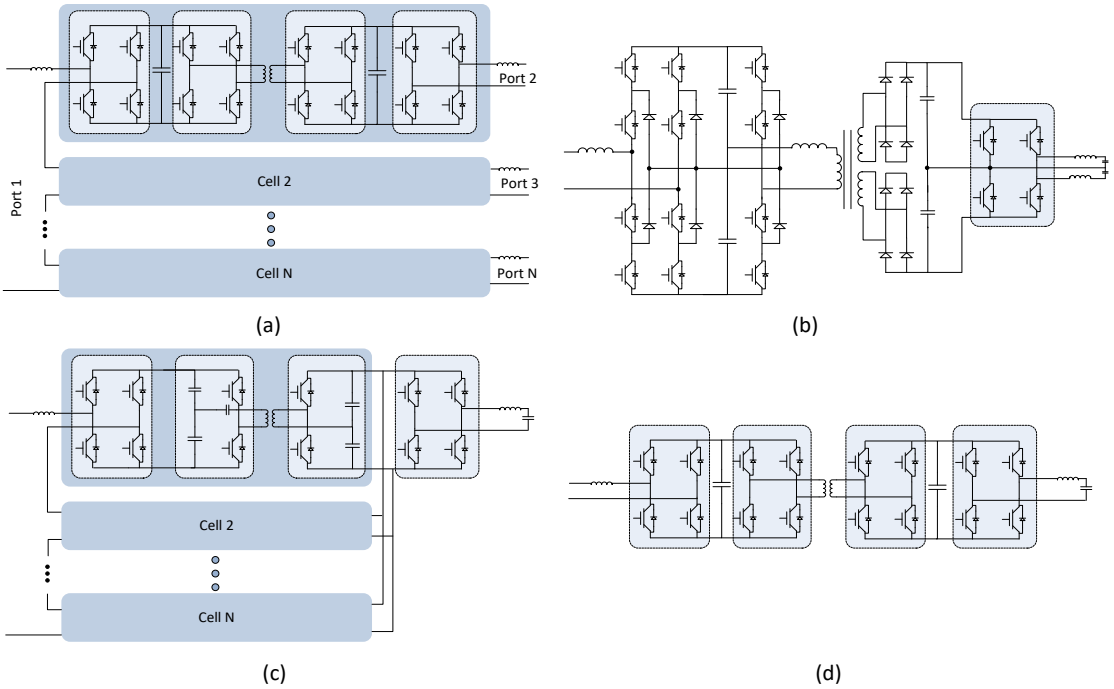


Figure 2: SST topologies (a) UNIFLEX (b) EPRI (c) ABB (d) GE

h-bridge converter structure. ABB uses a cascaded multilevel converter in the input of SST with a 15 kV grid for traction application. All four SST topologies [10] are shown in Figure 2. SST also provides more functionalities and benefits compared to the traditional transformer such as ac voltage and current as well as dc bus voltage regulation using power converter controllers while the traditional transformer has no such regulatory functionality. Moreover, IoT enabled inverters [11] can improve the monitoring, control, regulation, and security of the SST that can introduce a new form of the transformer as a smart transformer.

In this paper we have introduced a three-stage three-port SST with detailed modulation and control strategy. In addition, the literature review on different SST structures presented here will be the primary knowledge needed in understanding and design of SST model.

Three-Stage Three-Port SST:

The overall model design, modulation, and simulation techniques are shown in this section. A three-stage, three-port SST structure is shown in Figure 3. The high voltage rectifier (AC-DC stage) consists of a five-level cascaded H-bridge converter that increases the power density and connected to two separate high voltage dc-link capacitors that equally divide the power flow into two Dual Active Bridge (DAB) based DC-DC stage. The low dc voltage is then inverted into ac voltage with the fundamental frequency. Only the DC-DC stage comprises high-frequency signals. This proposed structure is developed for the distribution level application where the voltages are mainly used between 2.3 to 35 kV. Hence the high voltage and high frequency rated switching devices are very important for the reliable and efficient design of the distribution level SST. But for the high voltage rated devices are still not enough for the high-frequency application [12]. An attractive solution to this problem is to use a multilevel topology which allows using low voltage rated device in a high voltage level system. As a result, a high switching frequency can be applied that helps to reduce the size of discrete components. Moreover, the high operating frequency also provides a better solution for harmonic distortion. Manufacturers are currently developing high voltage rated devices with a possible increase in operating frequency which can also be used in a modular-based topology for very high voltage applications.

There are many multilevel topologies proposed by many researchers in the past [13],[14]. A five-level cascaded h-bridge (CHB) topology is used for the high voltage end of the SST in this paper. The switching devices are indicated as $S_{r1}, S_{r2}, S_{r3}, S_{r4}, S_{r5}, S_{r6}, S_{r7}, and\ S_{r8}$. Leg 1 consists of $S_{r1} and\ S_{r3}$ while leg 2, leg 3, and leg4 consist of S_{r2}, S_{r4}; S_{r5}, S_{r7}; and S_{r6}, S_{r8} respectively. Unlike the h-bridge topology, the PWM for CHB is slightly different. The carrier signals for leg 1 and leg 2 are shifted by 180 degrees whereas leg 3 and leg 4 are shifted by 90 degrees from leg 1 and leg 2 respectively. The CHB structure is shown in the rectifier stage of the SST. It is important to note that a phase-shifted carrier signal is used to generate PWM in this case. Table I shows the switching state for the CHB based rectifier of the SST. Only the first switches from each leg are considered in this table for the switching state representation while others being fully complementary to each other. Four carrier signals are required for four legs of the CHB structure while only two carrier signals are sufficient for the full-bridge converter. The phase-

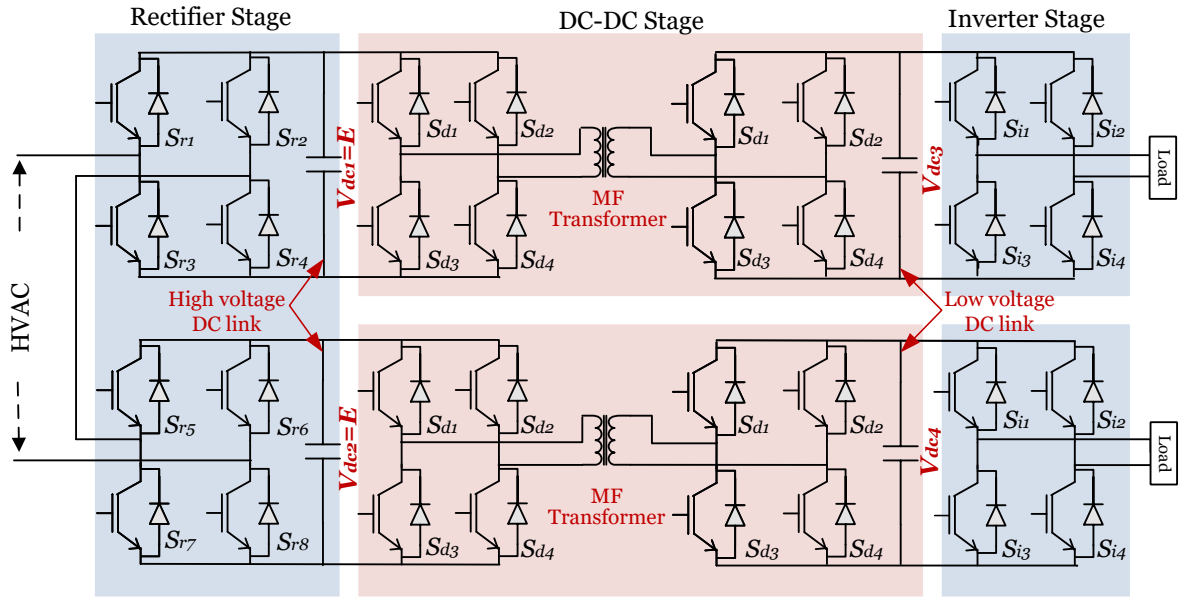


Figure 3: Three-stage three-port SST configuration.

Table I: Switching States for CHB

Switching State				Inverted Voltage
S_{r1}	S_{r2}	S_{r5}	S_{r6}	
1	0	1	0	**2E**
1	0	1	1	**E**
1	0	0	0	
1	1	1	0	
0	0	1	0	
0	0	0	0	**0**
0	0	1	1	
1	1	0	0	
1	1	1	1	
1	0	0	1	
0	1	1	0	
0	1	1	1	**-E**
0	1	0	0	
1	1	0	1	
0	0	0	1	
0	1	0	1	**-2E**

shifted carrier signal is compared with a reference signal to generate the PWM for the CHB rectifier. Figure 4 shows the PWM generation technique where cr. 1 to cr. 4 denotes carrier signals for leg 1 to leg 4. Cr. 2 is 180-degree phase-shifted from cr. 1 while the cr. 3 and cr. 4 are 90-degree shifted from the first two legs. Figure 4 (a) shows all four PWM generation technique whereas Figure 4 (b), (c), (d), and (e) present individual PWM technique that clearly shows the generation of pulse for each leg depends on the variable reference signal and the fixed carrier signal. On the other hand, the rest of the SST structure is developed based on a full-bridge converter structure which requires the same PWM technique as shown in Figure 4 except the required carrier signals are only 2 (180-degree phase-shifted) instead of 4.

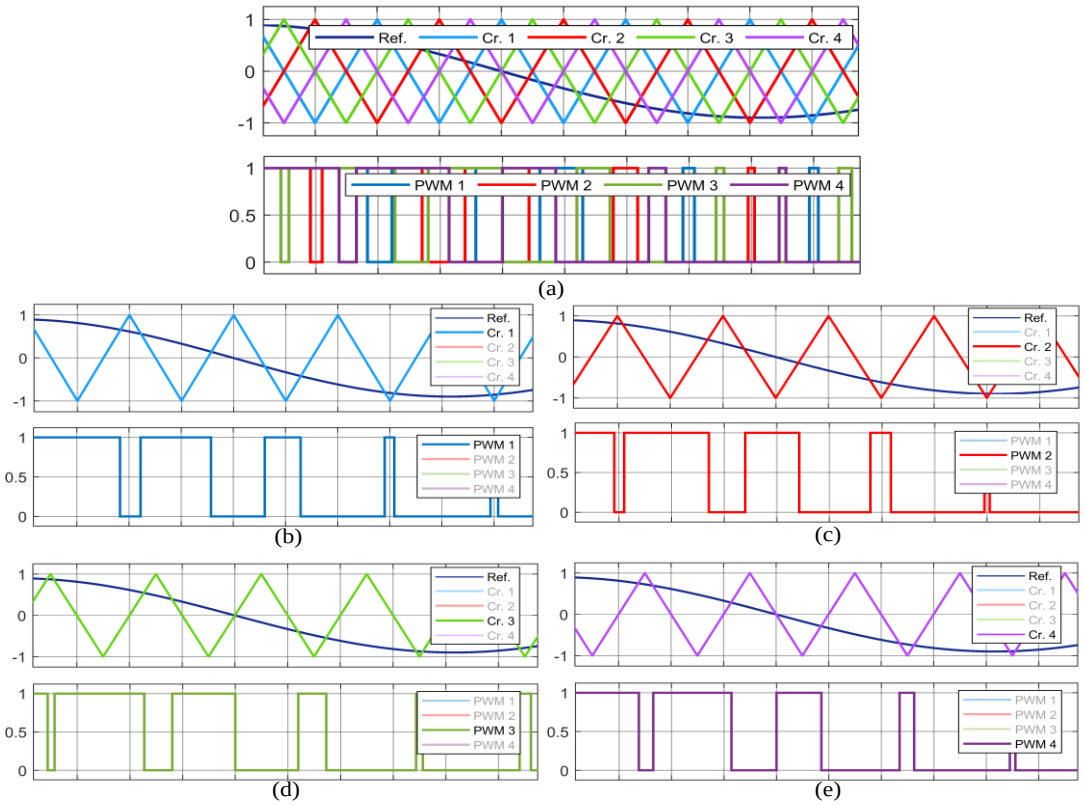


Figure 4: PWM generation technique for CHB.

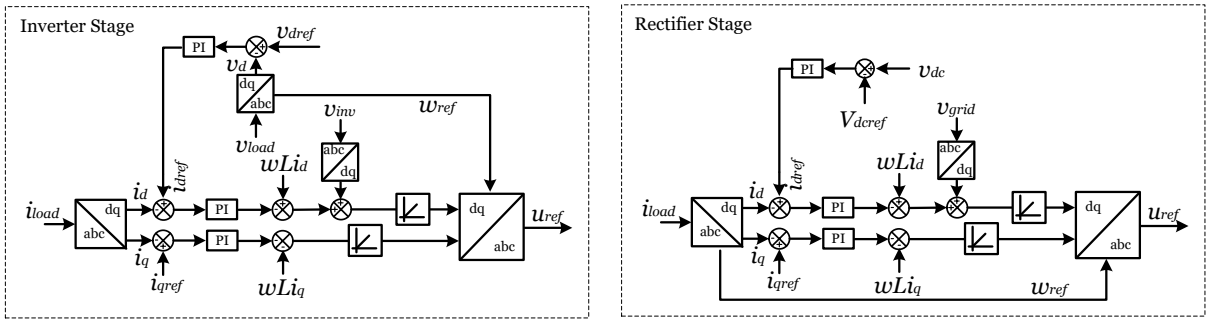
Control Strategy:

Upon successful development of the design and modulation of all power converters of SST, it is important to develop a control model to provide a reliable, resilient, and efficient SST for the grid application. The high and low voltage balancing operation across the DC bus capacitor has been very challenging for SST configuration especially for parallel-connected DAB and multi-port application [15]. In this paper, a d-q vector control-based DC voltage and load voltage balancing technique for both rectifier and inverter stages are presented. A simple classic d-q vector controller is applied in this system.

Rectifier Stage

The high voltage grid is connected to the front end of the SST that is configured with a CHB converter topology for high power density. The grid is connected through an LCL filter to remove unwanted harmonic distortions. The overall structure can be modeled into a mathematical equation applying a voltage distribution across each component which gives the equation (1).

$$V_{grid} = i_{grid}R + L\frac{di_{grid}}{dt} + v_{inv} \quad (1)$$



(a) (b)

Figure 5: Control structure for rectifier and inverter stages.

This equation can be expressed into a d-q matrix format in order to develop a controlled d and q component of grid voltage. The mathematical derivation is shown in (2) and (3),

$$\begin{bmatrix} v_{d_{grid}} \\ v_{q_{grid}} \end{bmatrix} = R \begin{bmatrix} i_{d_{grid}} \\ i_{q_{grid}} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{d_{grid}} \\ i_{q_{grid}} \end{bmatrix} + \omega L \begin{bmatrix} -i_{q_{grid}} \\ i_{d_{grid}} \end{bmatrix} + \begin{bmatrix} v_{d_{inv}} \\ v_{q_{inv}} \end{bmatrix} \tag{2}$$

$$\left.\begin{aligned} v_{d_{inv}} &= -\left[R i_{d_{grid}} + L \frac{d i_{d_{grid}}}{dt} \right] + \omega L i_{q_{grid}} + v_{d_{grid}} \\ v_{q_{inv}} &= -\left[R i_{q_{grid}} + L \frac{d i_{q_{grid}}}{dt} \right] - \omega L i_{d_{grid}} + v_{q_{grid}} \end{aligned}\right\} \tag{3}$$

Inverter stage

A similar technique is applied for the inverter stage with new and different control parameters. The generated inverter DQ-axis voltage and current from the abc to dq transformation are used by voltage and current loop controller that uses the d-q reference frame for the voltage and current loop control [16]. Applying KVL into the inverter circuit that consists of an LCL filter gives (4),

$$V_{inv} = i_{load} R + L \frac{d i_{load}}{dt} + v_{load} \tag{4}$$

Equation (5) can be transformed as a d-q matrix format shown in (5) and the further calculation can break down the equation into d and q frame shown in (6),

$$\begin{bmatrix} v_{d_{inv}} \\ v_{q_{inv}} \end{bmatrix} = R \begin{bmatrix} i_{d_{load}} \\ i_{q_{load}} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{d_{load}} \\ i_{q_{load}} \end{bmatrix} + \omega L \begin{bmatrix} -i_{q_{load}} \\ i_{d_{load}} \end{bmatrix} + \begin{bmatrix} v_{d_{load}} \\ v_{q_{load}} \end{bmatrix} \tag{5}$$

$$\left.\begin{aligned} v_{d_{load}} &= -\left[R i_{d_{load}} + L \frac{d i_{d_{load}}}{dt} \right] + \omega L i_{q_{load}} + v_{dinv} \\ v_{q_{load}} &= -\left[R i_{q_{load}} + L \frac{d i_{q_{load}}}{dt} \right] - \omega L i_{d_{load}} + v_{qinv} \end{aligned}\right\} \tag{6}$$

Using these mathematical models, the primary control algorithm for rectifier and inverter stages are developed and the schematic diagrams of the control system are presented in Figure 5. The generated reference signal from the output of the control system is then applied to the PWM generation block which uses the modulation technique presented previously in order to generate the required PWM for the rectifier and the inverter.

Simulation Results:

Figure 6 shows the simulation result of the three-stage three-port SST model. The main target is to maintain the HVDC and LVDC voltage using the converter in the rectifier stage and the inverter stage. Since the rectifier stage is developed using a CHB topology that uses one control unit, but the low voltage end is divided into two separate ports that require two individual control units with similar functionality as the operating conditions are similar. All the specifications are given in Table II. Figure 6 (a) and (b) shows the five-level voltage from CHB and the grid voltage across the filter capacitor. The controller uses two-loop controllers (voltage and current) to ensure equal power-sharing through both HVDC capacitors. The HVDC voltage across both capacitors are shown in Figure 6 (c) and (d) that achieved the voltage stability in less than 0.5 s. The primary and secondary inverted voltage for the transformer from respective converters in the dc-dc stage is also shown in Figure 6 (e), (f), (g), and (h). It can be noticed that these inverted signals are high-frequency signal that is not possible in traditional transformer application. On the other hand, the LVDC voltages are individually controlled by the inverter stage controller for the equal power sharing and stabilizing the ac load voltages which are shown in Figure 6 (i), (j), (k), (l), (m), and (n) where (k) and (l) are inverted outputs before the filter.

Table II: System Specifications.

Stage	Name	Value
Rectifier stage	Grid voltage (peak)	7200 V
	Filter	2 mH, 2.2 μF
	Operating frequency	60 Hz
	Switching frequency	10 kHz
	HVDC	5330 V
DC-DC stage	Operating frequency	2 kHz
	Switching frequency	20 kHz
	Transformer ratio	30:1
Inverter stage	LVDC	160 V
	Operating voltage	60 Hz
	Switching frequency	10 kHz
	Filter	10 mH, 3 μF

Students are expected to apply different system specifications for their simulation model with modified controller, based on the operating conditions. The comparison of this different simulation results will boost the understanding of the system performance in different scenarios.

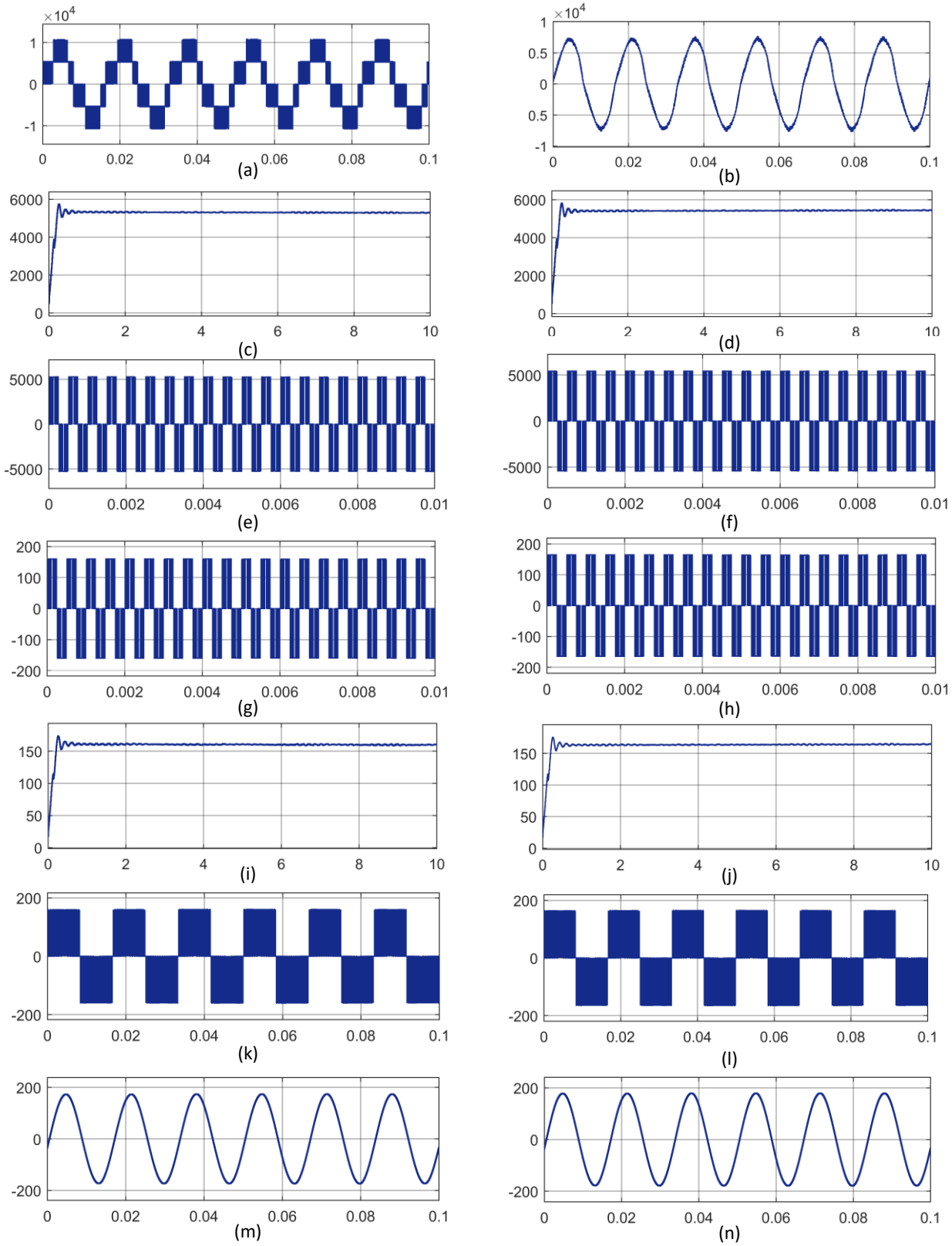


Figure 6: Simulation results. (all graphs are measured in the Voltage (V) unit)

Conclusion:

Two loop controller-based SST model with the three-stage three-port system is presented in this paper. This SST model uses a multilevel converter topology with high power capability. The controller uses the HVDC voltage from both rectifier stage capacitors to compare with the reference voltage and calculate the difference through a voltage and current loop in order to reach the voltage stability. The control method is validated in a MATLAB Simulink platform and the results are presented for the effectiveness and correctness of the system. The results will be incorporated in projects and labs for the upper-level undergraduate power electronics class to demonstrate the relevance and significance of our research in industry. Students will gain state-of-the-art experience in the laboratory before they graduate.

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